TouchSynth

An MCU-controlled analog monophonic synthesizer
on a single 4-layer board

Design report, revision 0.1

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Abstract

TouchSynth is a small monophonic analog synthesizer that is played on a capacitive touch keyboard and controlled entirely by a CH32V003/CH32V002 microcontroller. It has no potentiometers or mechanical switches. The sound path is fully analog:

- a timer-reset integrator oscillator (DCO),
- a four-pole transistor ladder filter with voltage-controlled resonance,
- a BJT differential-pair VCA with a firmware-calibrated offset trim.

All control voltages are generated by PWM and passive filters. The board uses only JLCPCB *Basic* and *Promotional Extended* parts; the MCU is hand-soldered from own stock.

This report documents the requirements, the circuit design and its justification by ngspice simulation (seven blocks plus the complete voice), a behavioural audio model, the 4-layer PCB, the bill of materials and the verification and validation plan, with the bring-up and functional test results of the first assembled board.

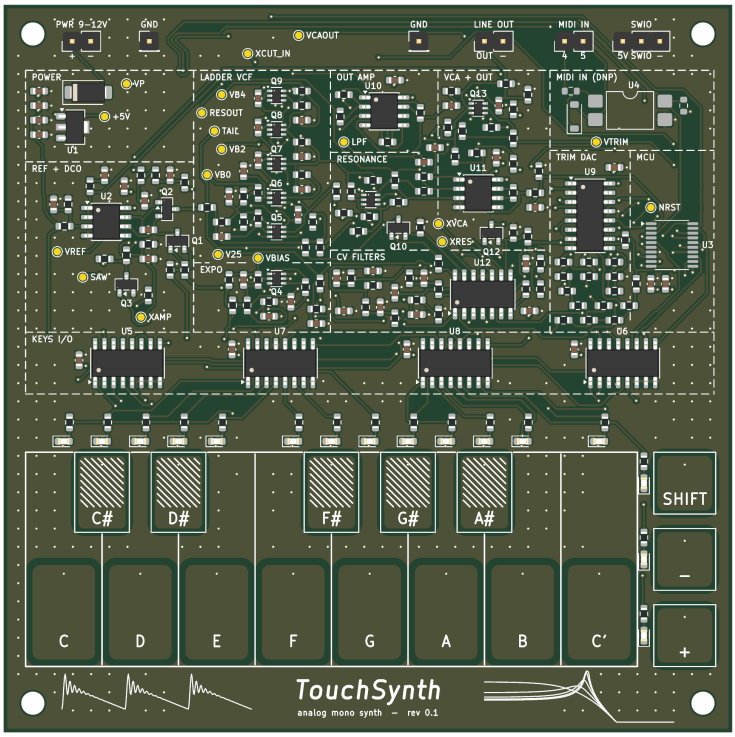


Figure 1: The board as ordered (rendered in KiCad 10), 100 × 100 mm, 4 layers.

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1 Introduction

1.1 Goal and constraints

The project had three aims:

1. Design a complete, self-contained electronic instrument end to end: requirements, circuit design, simulation, PCB layout and fabrication.
2. Keep the part count and the cost of assembly low.
3. Build in enough observability that the board can be verified automatically once it is back from the factory.

The following constraints shaped the design:

- **Parts**: only JLCPCB *Basic* and *Promotional Extended* parts, so there are no feeder loading fees and the board can be assembled in JLCPCB's economic PCBA service. The part lists were downloaded from the JLCPCB parts API (351 Basic and 1235 Promotional parts) and every BOM line was chosen from them.
- **MCU**: a CH32V003F4P6 or CH32V002F4P6 in TSSOP-20 from own stock, hand-soldered (do-not-populate in the assembly BOM). Both variants are pin compatible; one firmware supports both.
- **User interface**: no potentiometers and no mechanical switches. Thirteen capacitive keys (one octave C–C) plus three function pads (SHIFT, −, +), and 16 LEDs.
- **Power**: 9 . . . 12 V DC on a 2-pin header, reverse-polarity protected.
- **Scope**: a demonstrator. Some imperfections (power-on pop, filter temperature drift) are accepted explicitly rather than solved with additional parts. MIDI input is laid out but not populated.

1.2 Tool flow

The design was carried out with open tools and scripts, so every artefact can be regenerated (Table 1). A single Python description of the circuit (`hw/design.py`) is the source of truth: the schematic, the PCB netlist and the simulation cross-check are all derived from it.

Table 1: Tool flow and where each step lives in the repository.

Step	Tool	Files
Part selection	JLCPCB parts API	`parts/*.csv`
Circuit simulation	ngspice-42 (WSL), Python	`sim/s1_dco` … `sim/s7_power`, `sim/lib/voice.py`
Behavioural audio model	Python + numba	`sim/behav/`
Circuit description	Python	`hw/design.py` (242 parts, 166 nets)
Schematic	generated KiCad 10 schematic	`gen_sch2.py`, `layouts.py`, `draw.py` (in `hw/`)
Checks	kicad-cli ERC, netlist and simulation cross-check	`check_netlist.py`, `check_sim.py` (in `hw/`)
PCB	KiCad 10 Python API, Freerouting 1.9, own maze router	`hw/gen_pcb.py`, `hw/pcb_*.py`
Fabrication data	kicad-cli	`hw/fab.py`
Firmware	ch32fun (git submodule), riscv64-unknown-elf-gcc	`firmware/`

2 Requirements

Table 2 summarises the functional requirements (full text in `docs/spec.md`). Each requirement is traced to a simulation and to a hardware test in Section 11.

Table 2: Functional requirements.

Block	Requirement
DCO	Pitch from an MCU timer, range $\geq$ C1 (32.7 Hz) … C7 (2093 Hz); saw amplitude constant within $\pm 5\,\%$ over the range
Waveforms	saw, pulse with variable width, sub-oscillator (-1 octave square), noise; each switchable
VCF	24 dB/oct transistor ladder; cutoff 30 … 15 000 Hz via a hardware exponential converter; resonance from zero to self-oscillation
VCA	≥ 70 dB attenuation when closed; envelope from firmware; CV feed-through nulled by a calibrated trim
Output	line level $\approx 1\,V_{pp}$ into $\geq 10\,k\Omega$, AC coupled
Control voltages	4 PWM channels, 12-bit effective resolution; ripple < -70 dB of full scale; settling $<$ 2 ms
Touch	16 pads; full scan ≥ 200 Hz; touch signal $\geq 5\times$ noise
Power	9 … 12 V, reverse protected, ≤ 60 mA
Test	audio loopback to the MCU ADC; test points; programming/debug over SWIO

3 System architecture

Figure 2 shows the architecture:

- **Audio path** (top row): analog from the oscillator to the line output.
- **MCU**: generates the oscillator timing and the waveform bits directly. The four continuous parameters (oscillator amplitude, cutoff, resonance, VCA level) are PWM outputs of TIM1, smoothed by passive three-pole filters and converted to currents.
- **Touch pads**: read through two CD4051 multiplexers with the ADC charge-slope method.
- **Shift-register chain**: three 74HC595 drive the 16 LEDs and an 8-bit R-2R DAC that trims the VCA offset.
- **Loopback**: a divided copy of the output returns to an ADC pin. It is used for self-test and calibration.

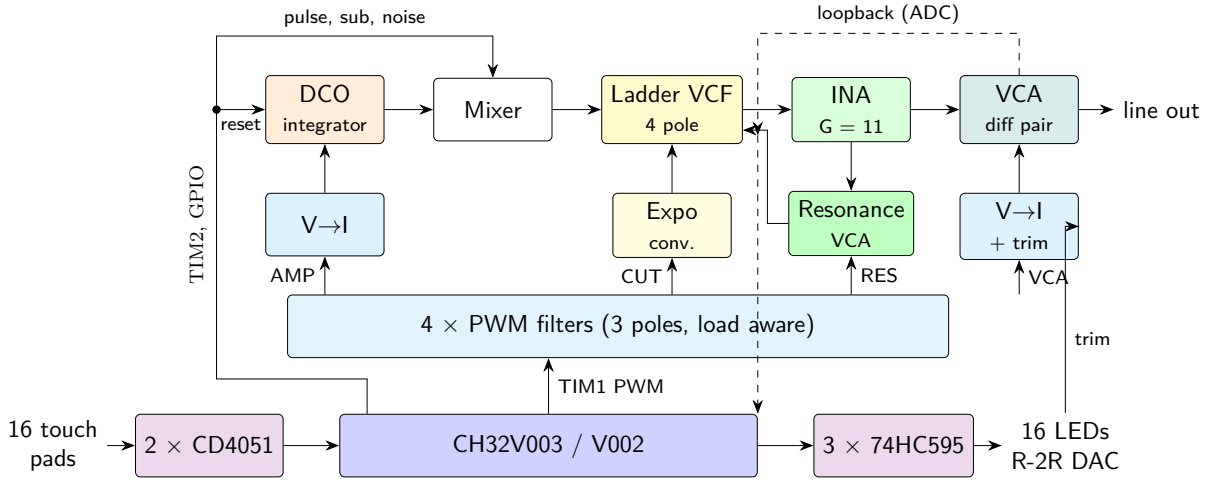


Figure 2: System architecture. The audio path is analog; the MCU sets all parameters through PWM control voltages and timing, and observes the output through the loopback.

3.1 Control concept

- **Oscillator timing**: TIM2 CH1 produces one short reset pulse per period, so the pitch is as exact as the 48 MHz timer. The saw amplitude is kept constant by making the integrator charging current proportional to the frequency (CV_{AMP}).
- **Waveform bits**: the pulse wave comes from TIM2 CH2. The sub-oscillator is a GPIO toggled in the TIM2 update interrupt, and noise is a GPIO driven by a firmware LFSR.
- **Control voltages**: TIM1 CH1–CH4 run at 10 bit and 46.9 kHz. The compare registers are updated by DMA bursts with 2-bit sigma-delta dithering, which gives 12-bit effective resolution at a high carrier frequency.
- **Firmware control loop**: envelopes, LFO, glide and the arpeggiator run in firmware at a 1 kHz control rate.

3.2 MCU pin assignment

Table 3 lists the pin map. The LED/DAC shift registers share the DATA and CLOCK lines with the multiplexer select lines S0 and S1, so no third multiplexer is needed.

Table 3: MCU pin map (TSSOP-20, identical for CH32V003 and CH32V002).

Pin	Port	Function	Pin	Port	Function
1	PD4	74HC595 LATCH	11	PC1	SUB oscillator (GPIO)
2	PD5	ADC A5 ← audio loopback	12	PC2	TIM2 CH2 → PULSE
3	PD6	USART RX ← MIDI	13	PC3	mux S0 / 595 DATA
4	PD7	NRST	14	PC4	mux S1 / 595 CLK
5	PA1	touch mux B → ADC A1	15	PC5	TIM2 CH1 → DCO reset
6	PA2	touch mux A → ADC A0	16	PC6	TIM1 CH1 → CV_{AMP}
7	VSS	GND	17	PC7	TIM1 CH2 → CV_{CUT}
8	PD0	NOISE (GPIO)	18	PD1	SWIO
9	VDD	+5 V	19	PD2	mux S2
10	PC0	TIM1 CH3 → CV_{RES}	20	PD3	TIM1 CH4 → CV_{VCA}

4 Circuit design

The complete schematic (7 hierarchical sheets) is reproduced in Appendix A. This section explains each block and its key values. Unless noted, all resistors are 1 % thick film 0603, and all capacitors are X7R/X5R 0603.

4.1 Power and references

- **Input**: an SS14 Schottky diode protects against reverse polarity. The protected rail V+ (8.6 . . . 11.6 V) supplies the analog circuitry.
- **+5 V**: a 78L05 supplies the MCU, the multiplexers, the shift registers and the LEDs.
- **Audio reference**: VREF = 4.5 V is derived from +5 V (1 kΩ/9.1 kΩ divider, 10 µF) and buffered by a TL072 follower. The follower has a 10 Ω + 1 µF output snubber instead of a bare capacitor. The simulation showed that the snubber is required for stability, see Section 5.
- **Other references**: VBIAS = 1.5 V and V25 = 2.5 V are plain dividers from +5 V. Referencing everything that sets pitch or cutoff to +5 V, not to V+, makes the sound independent of the input voltage.

4.2 Oscillator (DCO)

The oscillator is a TL072 inverting integrator ($C_{\text{int}} = 10\,\text{nF}$) whose non-inverting input sits at VREF (Figure 3):

- **Charging**: a V→I converter (LM324 + MMBT3904, $R_E = 33\,\text{k}\Omega$) draws the charging current from the summing node, so the saw ramps up from 4.5 V.
- **Reset**: once per period a 3 µs pulse from TIM2 CH1 goes through an MMBT3904 level shifter to a 2N7002 across the capacitor. A 2.2 kΩ gate resistor softens the charge-injection spike.
- **Constant amplitude**: the firmware sets $I = A\,C_{\text{int}}/(T - t_{\text{reset}})$, so the saw amplitude A does not depend on the period T.

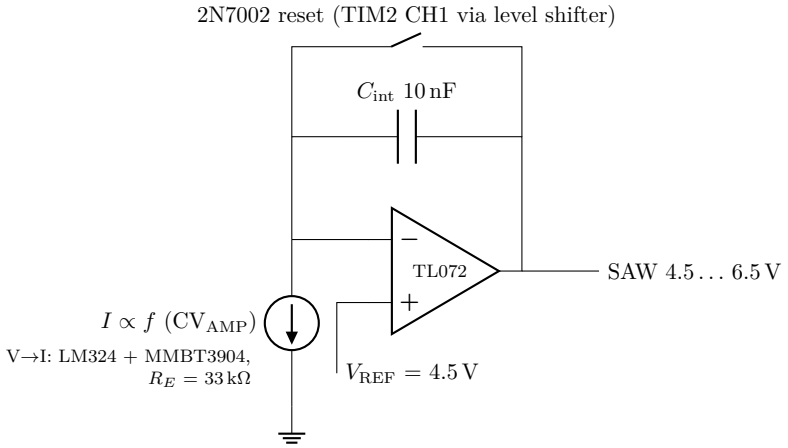


Figure 3: DCO core (simplified): integrator with current-sink charging and a MOSFET reset switch.

Mixer. The saw (150 kΩ), pulse, sub and noise (470 kΩ each) are summed into 10 kΩ to the ladder input bias VB0 through 1 µF.

4.3 Control-voltage filters

Each TIM1 PWM output is smoothed by three RC poles (Figure 4):

- **LIN networks** (CV$_{\text{AMP}}$, CV$_{\text{RES}}$, CV$_{\text{VCA}}$): the last stage is a $4.7\,\text{k}\Omega/15\,\text{k}\Omega \parallel 22\,\text{nF}$ divider into an LM324 V→I converter. The DC ratio is 0.591.
- **EXP network** (CV$_{\text{CUT}}$): the last stage is a $33\,\text{k}\Omega/1.5\,\text{k}\Omega \parallel 100\,\text{nF}$ divider to VBIAS. It drives the exponential converter base directly, with a ratio of 0.0373 (10.4 octaves over the 5 V PWM range).

Both ratios include the series resistance of the first two stages; Section 5.10 describes the bug that made this explicit.

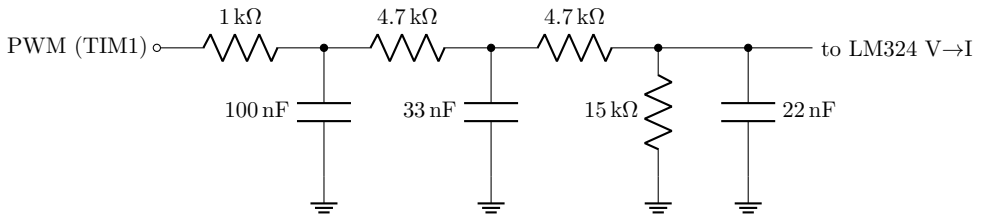


Figure 4: LIN control-voltage network. The EXP variant (CV$_{\text{CUT}}$) replaces the last stage by $33\,\text{k}\Omega$ / $1.5\,\text{k}\Omega \parallel 100\,\text{nF}$ to VBIAS.

4.4 Ladder filter, exponential converter and output amplifier

- **Ladder**: a Moog-type ladder made of five BC847BS dual NPN transistors (input pair, three rungs, load pair) and four 33 nF capacitors.
- **Bias chain**: a divider from V+ (2.2 kΩ, 4×1 kΩ, 2.4 kΩ, each tap decoupled with 10 µF) sets the base voltages VB0 … VB4.
- **Exponential converter**: the tail current comes from a BC847BS pair with an LM324. The reference current is 8.3 µA through 300 kΩ, and the loop is compensated with 1 nF.
- **Output amplifier**: the differential output across the top capacitor is read by a TL072 two-op-amp instrumentation amplifier (gain 11, output referenced to VREF). Its JFET inputs do not load the ladder, whose source impedance reaches about 50 kΩ at low cutoff.

4.5 Resonance

The resonance loop is a voltage-controlled amplifier of its own:

- **Input**: the filter output is attenuated 1:13 and AC coupled into a BC847BS differential pair.
- **Gain control**: the pair's tail current comes from CV_{RES} through an LM324 V→I converter ($R_E = 6.2\,k\Omega$).
- **Feedback**: the collectors feed a TL072 unity difference amplifier. Its output returns through 4.7 µF and 22 kΩ into the second input of the ladder.

The difference amplifier removes the common-mode step of the collectors when the tail current changes. An earlier single-ended version injected volt-level DC steps into the ladder.

4.6 VCA, trim DAC and output

- **Core**: a BC847BS differential pair (bases biased from VREF, input attenuated 1:34) with 4.7 kΩ collector resistors. A TL072 difference amplifier (10 kΩ/22 kΩ) follows, then 10 µF to the line output.
- **Tail current**: an LM324 V→I converter ($R_E = 4.7\,k\Omega$) supplies it. A 470 kΩ resistor from +5 V to the emitter makes the current truly zero at CV = 0 despite the op-amp offset voltage.
- **Offset trim**: the third 74HC595 in the LED chain drives an 8-bit R-2R DAC (100 kΩ/200 kΩ). The DAC injects a small offset current into one base (1 MΩ, with 2 MΩ fixed on the other base). The firmware finds the DAC code that nulls the CV feed-through ("thump").
- **Loopback**: a 10 kΩ/15 kΩ divider with 1 nF feeds the output to PD5 (ADC A5).

4.7 Touch keyboard, LEDs and MIDI

- **Touch pads**: the 16 pads are copper under solder mask (white keys 8.6 mm × 13 mm, black keys 6.5 mm × 10 mm, function pads 7.5 mm square). Each group of eight goes through a CD4051 to one ADC channel.
- **Measurement**: the ch32fun ADC slope method (`extralibs/ch32v00x_touch.h`) measures each pad.
- **LEDs**: each of the 16 red 0603 LEDs has its own 4.7 kΩ series resistor (about 0.6 mA).
- **MIDI**: an LTV-817 optocoupler feeds the USART RX pin. These parts are not populated; the footprints are kept.

5 Simulation

5.1 Method

- **Simulator**: every block was simulated in ngspice-42, driven by Python scripts. The shared netlist fragments are in `sim/lib/voice.py`, so all simulations use identical circuits.

- **Models**: TI Boyle macromodels for the TL072 and LM324, NXP Gummel-Poon models for the BC847B, generic MMBT3904 and 2N7002 models, and a behavioural 78L05.
- **Supply corners**: V+ = 8.6 V and 11.6 V.
- **Firmware in the loop**: the firmware is modelled where it matters. Timer periods are quantised at 48 MHz, the CVs are 12-bit codes, and the control rate is 1 kHz.
- **Calibration data**: calibrations found by one simulation (DCO gain, cutoff table, VCA law, resonance threshold) are written to CSV files and read back by the others, never copied by hand.
- **Cross-check**: `hw/check_sim.py` verifies that the 145 simulated components match the schematic values.

Table 4 summarises the results. All blocks meet their requirements.

Table 4: Simulation summary.

#	Block	Requirement	Result	Status
S1	DCO	amplitude flat ±5 %, C1–C8, 9 . . . 12 V	−2.2 / +0.8 %, supply independent	pass
S2	CV filters	ripple < −70 dB FS, settling < 2 ms	−81 / −84 dB; 1.3 / 1.2 ms (1 %)	pass
S3	Ladder VCF	30 . . . 15 000 Hz, 24 dB/oct, self-oscillation	19.9 . . . 19 800 Hz, −23 dB/oct, self-osc. from $CV_{RES} \approx 3.1$ V	pass
S4	VCA	≥ 70 dB off, low feed-through	121 dB; thump 94–101 mV → < 0.6 mV after trim	pass
S5	Touch	Δ ≥ 5× noise, ≥ 200 Hz	SNR 39 (V003) / 152 (V002) worst case; 1.4 kHz scan	pass
S6	Full voice	plausible sound, loopback in range	1.22 V_{pp} line out; loopback 2.3 . . . 2.9 V	pass
S7	Power	9 . . . 12 V, ≤ 60 mA, low hum	31 / 32 mA; hum −81 dB	pass

5.2 S1 – Oscillator

Figure 5 shows the saw waveforms and the reset. Figure 6 shows the amplitude versus the note.

- **Ramp**: rises from 4.53 V to 6.50 V. The −2.2 % gain error is removed by one calibration constant.
- **Flatness**: over C1–C8 and both supply corners it stays within −2.2 %/0.8 %. The low end is limited by the 12-bit quantisation and the LM324 offset.
- **Reset**: completes in about 2.5 µs. Charge injection leaves a 0.43 V, 100 ns spike, which is negligible against the 2 V reset step.

5.3 S2 – Control-voltage filters

The first iteration used 12-bit PWM at 11.7 kHz. It reached only −66.7 dB ripple and 2.2 ms settling. Switching to 10-bit PWM at 46.9 kHz with 2-bit sigma-delta dithering keeps 12-bit resolution and moves the carrier up by a factor of four.

Table 5: S2 results at the worst-case duty cycle (50 %), dither active.

Channel	Full scale	Ripple	re FS	Settling 1 %	Settling 0.1 %
LIN	2.95 V	271 μV_{pp}	−81 dB	1.31 ms	1.88 ms
EXP	187 mV	12 μV_{pp}	−84 dB	1.22 ms	1.68 ms

The EXP ripple corresponds to 0.8 cent of cutoff modulation.

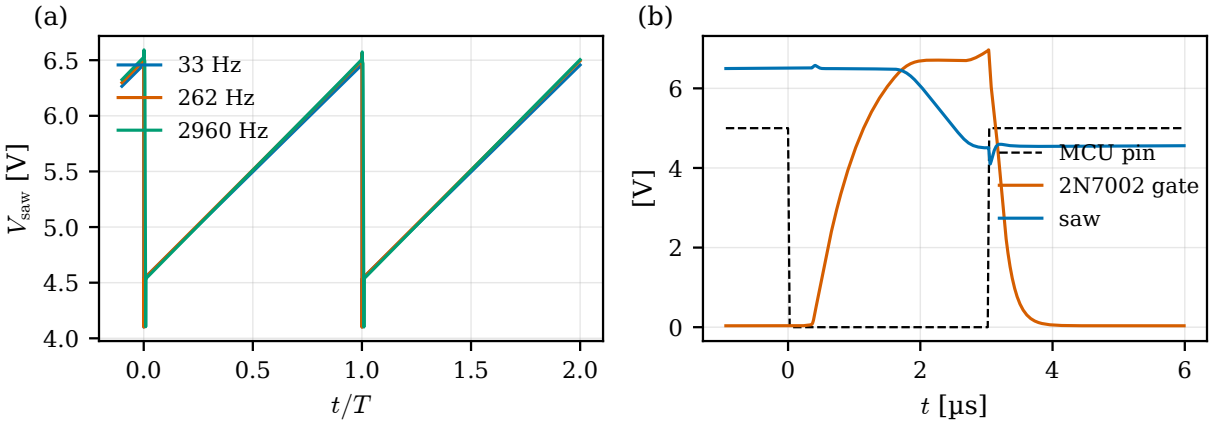


Figure 5: S1: (a) saw at 33 Hz, 262 Hz and 2.96 kHz over two periods (time normalised to the period); (b) reset detail at 4.19 kHz: MCU pin, 2N7002 gate and saw.

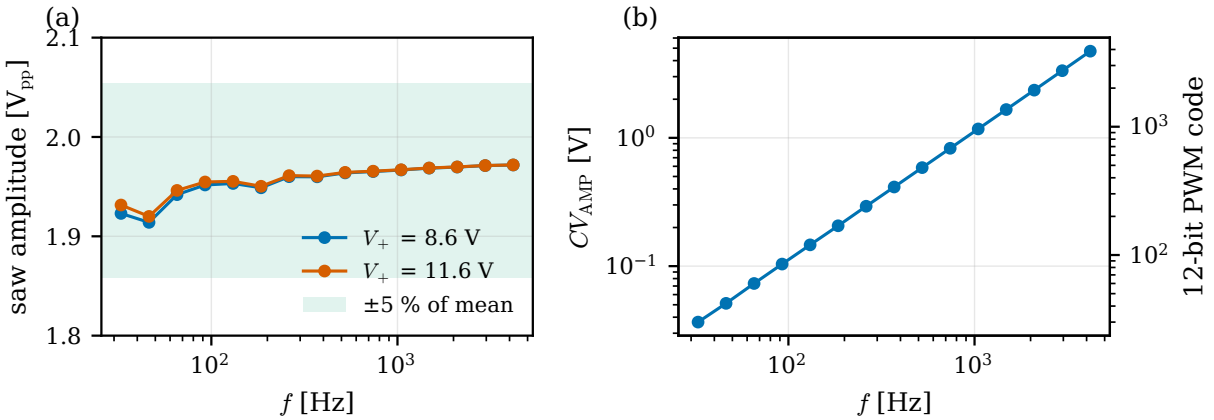


Figure 6: S1: (a) saw amplitude versus note at both supply corners; (b) firmware CV_{AMP} law and 12-bit code.

5.4 S3 – Ladder filter

5.5 S4 – VCA

- **Gain**: maximum 7.4 dB. THD is 0.06 / 0.21 / 0.81 % at 0.3 / 0.6 / 1.2 V_{pp} input.
- **Off attenuation**: 121 dB. Without the 470 kΩ anti-offset resistor a 7 mV LM324 offset would leave only 52 dB.
- **Feed-through**: with realistic mismatch (±1 % collector resistors, 1 . . . 2 mV V_{BE} offset) the CV feed-through is 94–101 mV per note, an audible thump. Both error terms scale with the tail current, so one static offset trim cancels both. After the two-point calibration the residual is 0.58 mV and 0.08 mV in the two mismatch cases.

5.6 S5 – Touch sensing

- **Model**: the ch32fun slope method. The pin is released to the internal pull-down, and the ADC sample-and-hold samples the first 0.625 µs of the decay. The model includes the multiplexer (30 pF common capacitance, 470 Ω on-resistance), the trace and the pad.
- **Sensitivity**: the multiplexer costs about a factor of five in sensitivity compared with a direct pin, but the margin stays large. A 5 pF touch gives 14.8–20.8 LSB per sample (V003) or 57–81 LSB (V002). The worst-case SNR is 39 and 152 with 16 samples per pad.
- **Scan rate**: a full scan takes 0.69 ms (1.4 kHz).

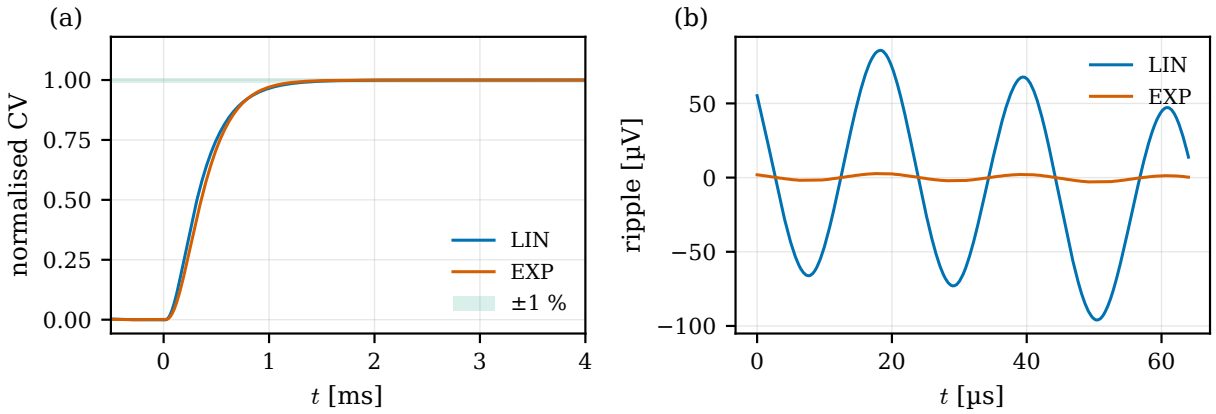


Figure 7: S2: (a) normalised 10 . . . 90 % step response; (b) steady-state ripple at 50 % duty with dither.

Table 6: S3 results.

Quantity	Value
−3 dB cutoff range (CV_{CUT} 0–5 V)	19.9 . . . 19 800 Hz (≈ 10 octaves)
Tracking	2.05 oct/V, log-linear
Slope (one octave above cutoff)	−23.1 dB/oct
Passband gain (ladder in → INA out)	20.4 dB, flat within 1.6 dB
Resonance peak at CV_{CUT} = 2.5 V	4.8 / 13.6 / 20.7 / 28.9 dB at CV_{RES} = 1 / 2 / 2.5 / 2.8 V
Self-oscillation threshold	CV_{RES} ≈ 3.1 V; 0.11 . . . 0.29 V_{pp} (soft-limited)
Supply sensitivity	+19 cent between 9 V and 12 V input
Temperature drift	−13.4 cent/K (accepted, see Section 12)

5.7 S6 – Complete voice

The complete analog circuit was simulated with the firmware behaviour modelled in Python:

- quantised timer periods,
- a sub-oscillator toggled once per period,
- a pulse-width LFO,
- ADSR envelopes,
- all CVs mapped through the calibrations of S1, S3 and S4.

The score is an eight-note bass line with filter envelope, followed by a held note with a slow resonant sweep. The line output peaks at 1.22 V_{pp}. The loopback node stays within 2.34 . . . 2.88 V, well inside the ADC range.

5.8 S7 – Power and references

- **Ripple**: with 200 mV_{pp} of 100 Hz ripple on the input, the line-output hum is −81 dB relative to 1.33 V_{pp} at both 9 V and 12 V.
- **Current**: 31 and 32 mA at 9 and 12 V, including an assumed 15 mA for the MCU, logic and LEDs. (Revision 0.1 of this report gave 33 and 42 mA from two model errors that partly cancelled: the 78L05 model drew only its quiescent current from the input, and the TL072 macromodel drew about 4 mA per amplifier instead of 1.4 mA. Both were found at bring-up, Section 11; the corrected model matches the measured 25 mA of board 1 within 1 mA.)
- **VREF buffer history**: the first VREF buffer (TL072 driving 10 µF through 100 Ω outside the loop) let 1.1 mV_{pp} of hum through, −47 dB at the output. A dual-loop variant fixed the hum but had a 48 Ω impedance peak. The final plain follower with an RC snubber has 5 mΩ at 100 Hz and a single well-damped peak.
- **Power-on pop**: about 3 V, decaying in about 0.3 s. It is accepted: switch the synth on

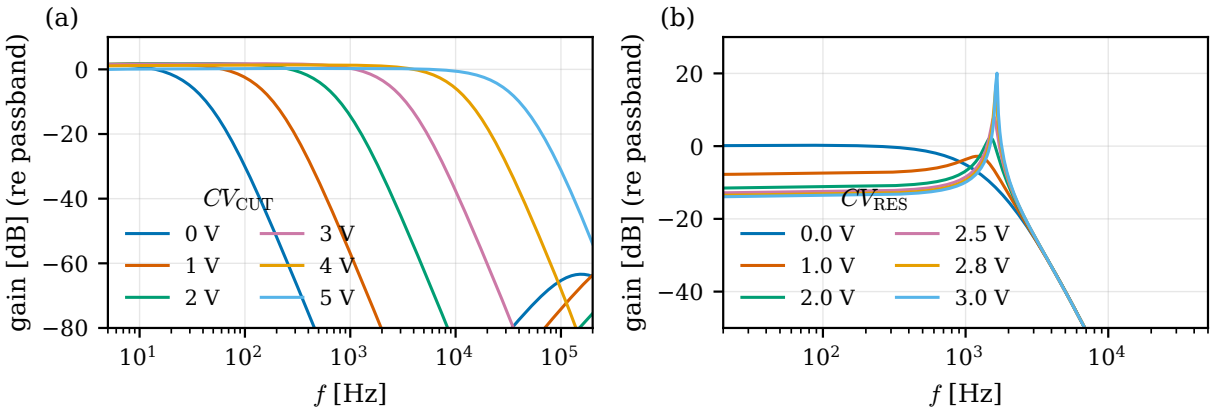


Figure 8: S3: (a) filter response for $\mathrm{CV_{CUT}} = 0$–$5\,\mathrm{V}$ without resonance; (b) response at $\mathrm{CV_{CUT}} = 2.5\,\mathrm{V}$ for $\mathrm{CV_{RES}}$ below the self-oscillation threshold.

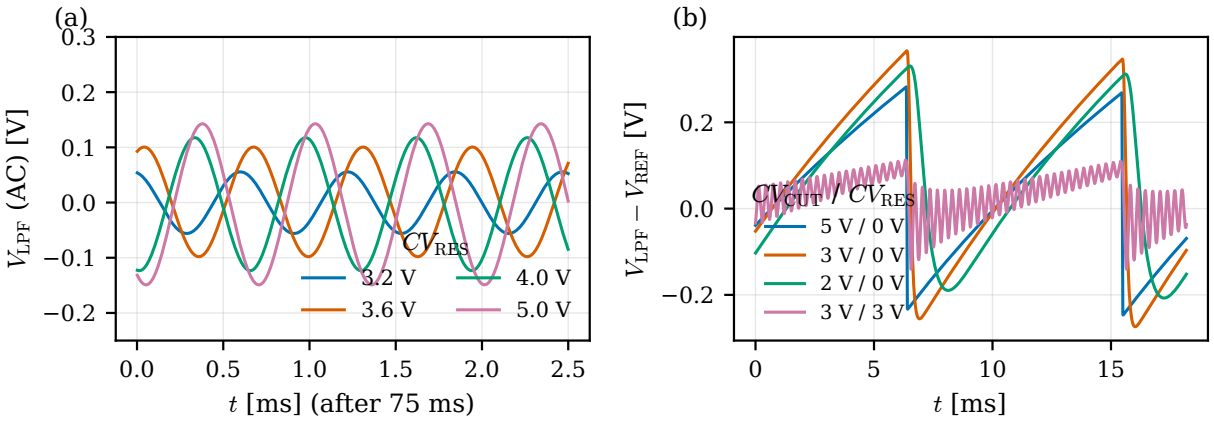


Figure 9: S3: (a) steady-state self-oscillation for several $\mathrm{CV_{RES}}$ above threshold; (b) 110 Hz saw through the filter at different cutoff and resonance settings.

before the amplifier.

5.9 S8 – Pulse output as PWM DAC

S8 (`sim/s8_dac/`) checks the DAC mode of Section 10.5 on the real netlist from the pulse input through mixer, ladder, VCA and line out, with the DCO held in reset. A 1 kHz test tone at −3 dBFS is encoded exactly as the firmware does it: 15.625 kHz samples, 8-bit duty with first-order error feedback. Three PWM variants are compared with an ideal DAC of the same scale, a continuous source that interpolates linearly between the samples (Table 7):

- **edge, hold**: TIM2 counting up at 187.5 kHz, each sample held for 12 periods (the first firmware version);
- **centre, hold**: TIM2 counting up and down at 93.75 kHz, so the pulses are centred in the period; each sample held for 6 periods;
- **centre, interpolated**: in addition, the duty is interpolated linearly from the previous sample over the 6 periods (the firmware).

Results:

- **Second harmonic**: with edge-aligned PWM the pulse centre moves with the duty, so the signal also modulates the pulse position. That adds a second harmonic at −45 dB (0.6 %). Centred pulses remove it: −68 dB, as clean as the ideal DAC. The third harmonic comes from the ladder itself in all cases.
- **Images**: holding each sample leaves images at $f_s \pm f$, −26 dB at a 20 kHz cutoff. Linear

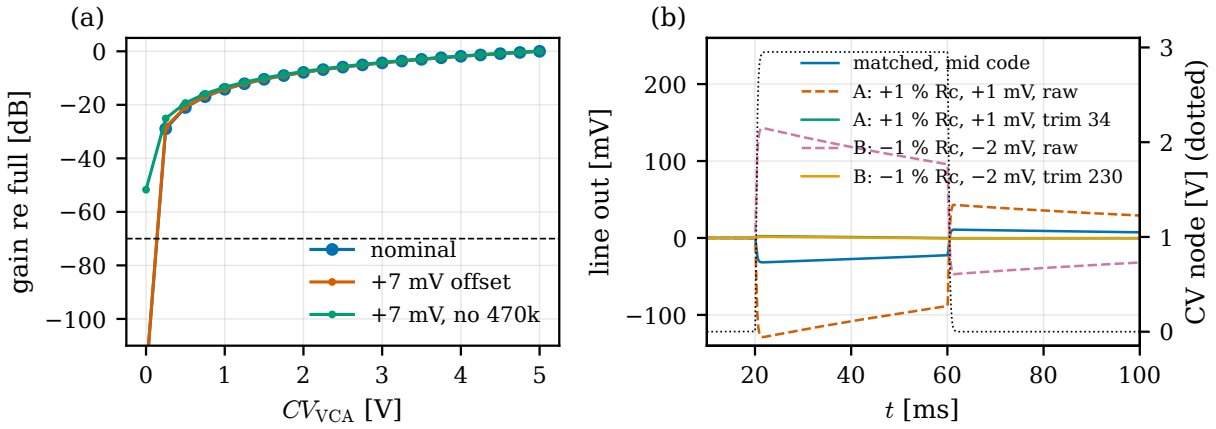


Figure 10: S4: (a) gain versus CV_{VCA} (nominal, with 7 mV op-amp offset, and without the anti-offset resistor); (b) CV feed-through for a 0 → full-scale step without signal, before and after the trim calibration.

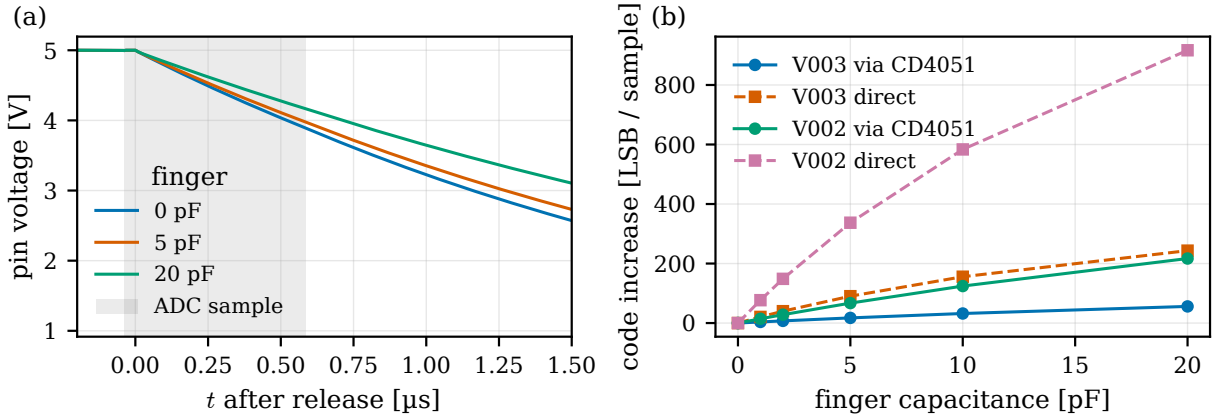


Figure 11: S5: (a) pin voltage after release for 0, 5 and 20 pF finger capacitance; (b) ADC code increase per sample versus finger capacitance, through the multiplexer and direct.

interpolation lowers them by 23 dB to the level of the ideal DAC.

- **Carrier**: halving the carrier to 93.75 kHz for the centred pulses leaves it 28 dB below the tone with the filter fully open. It is ultrasonic and falls below −74 dB at cutoffs of 5 kHz and lower (the kettle uses 4 kHz).
- **Noise**: without the images, −52 … −56 dB in the audio band, about the board's own noise floor. The level matches the ideal DAC within 0.4 dB.

5.10 Design changes found by simulation

Table 8 lists every change that the simulations caused. The most instructive was the *CV network loading* bug:

- **The bug**: the last RC stage of each control-voltage filter was designed as a divider for an ideal source, but it sits behind the series resistance of the first two stages. The real LIN ratio was therefore 0.36 instead of 0.6, and the cutoff range shrank to 44 … 4000 Hz.
- **Why the block tests missed it**: the individual block simulations had driven the dividers with ideal voltages.
- **How it was found**: only when the behavioural model (Section 6) could not match the full-voice simulation.
- **Fix**: all networks were redesigned with the loading included, and every simulation now drives the CVs through the real networks.

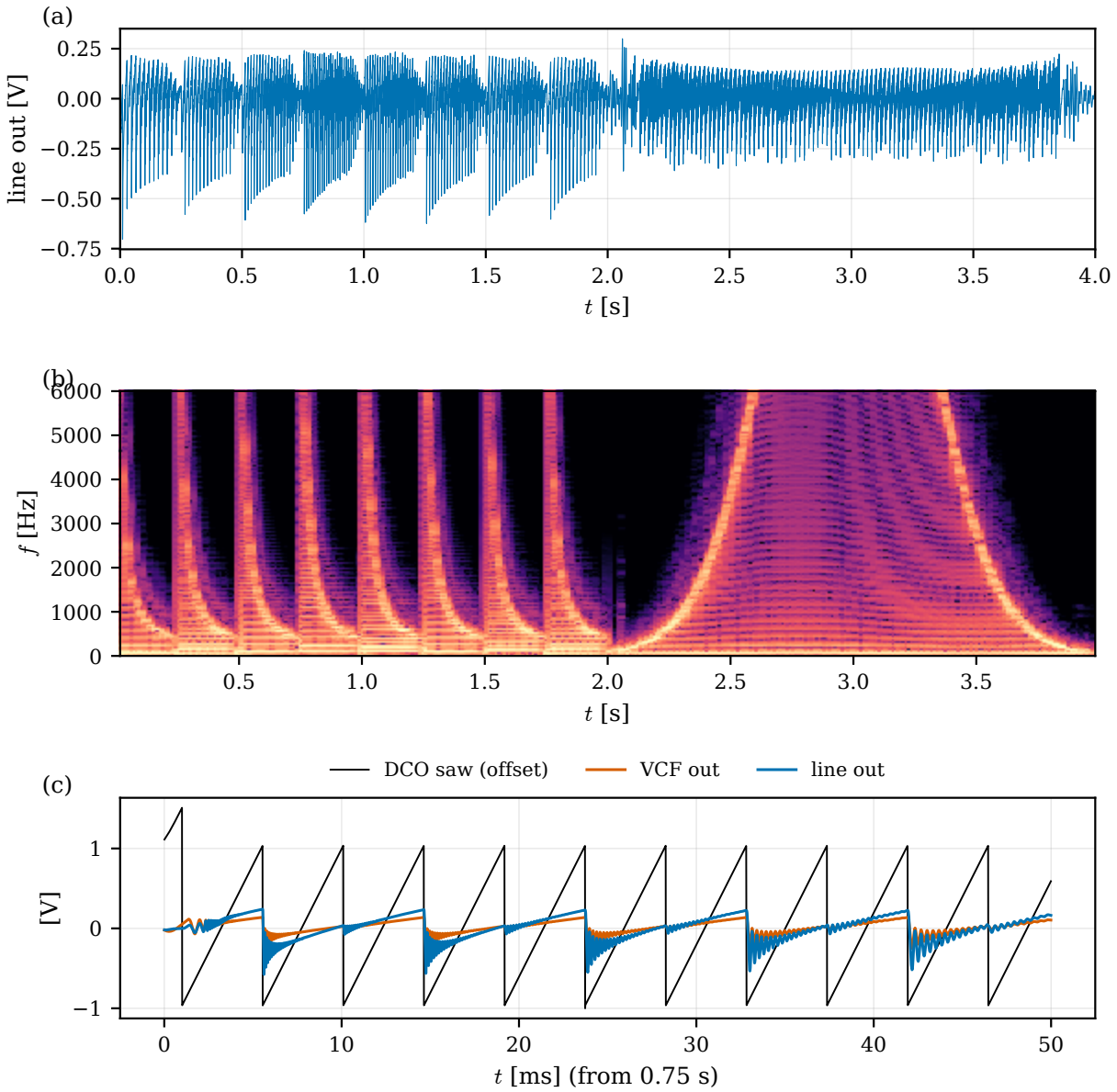


Figure 12: S6: (a) line out; (b) spectrogram; (c) detail at 0.75 s: DCO saw, filter output and line out.

6 Behavioural model and audio

A fast Python/numba model of the voice (`sim/behav/`) renders audio in seconds instead of the minutes ngspice needs. It mirrors the hardware split:

- **Firmware layer**: patch parameters, envelopes, LFO, glide, accent and slide, timer quantisation, 12-bit CVs at 1 kHz.
- **Analog layer** at 192 kHz: band-limited oscillators (polyBLEP), the S2 filters, a tanh ladder, the VCA law and the output coupling.

The model's constants are taken from the ngspice results. The resonance loop gain was obtained by inverting the S3 resonance peaks. Two parameters were fitted to the self-oscillation pitch and amplitude.

Compared with ngspice on the S6 score, the model matches:

- the level within −0.6 dB (1.1 dB rms),
- the self-oscillation pitch within 2 % and its amplitude within 7 %,
- the overall brightness (spectral centroid) within 300 cent; the difference is concentrated where

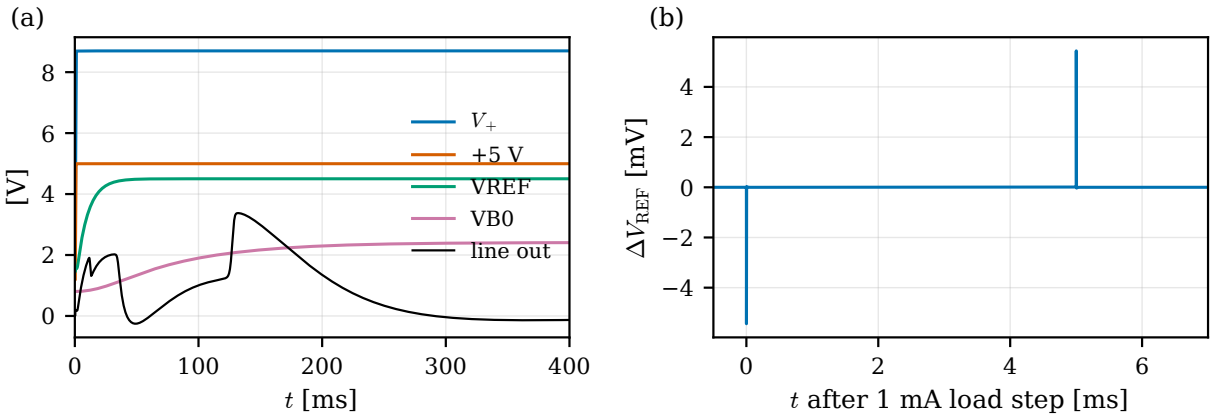


Figure 13: S7: (a) power-up at 9 V; (b) VREF response to a 1 mA load step.

Table 7: S8: 1 kHz at −3 dBFS through the pulse input, three PWM variants and an ideal DAC (`docs/results/s8_dac.csv`); levels relative to the 1 kHz tone. The firmware uses *centre, interpolated*.

Cutoff	Source	1 kHz [mV]	H2 [dB]	H3 [dB]	Image [dB]	Carrier [dB]	Noise [dB]
20 kHz	edge, hold	292	−45	−47	−26	−53	−43
	centre, hold	292	−68	−47	−27	−28	−50
	centre, interpolated	290	−69	−47	−49	−28	−52
	ideal	295	−66	−55	−50	–	−49
5 kHz	edge, hold	348	−46	−42	−43	−87	−55
	centre, hold	348	−66	−42	−43	−74	−56
	centre, interpolated	346	−67	−42	−66	−74	−56
	ideal	359	−65	−43	−67	–	−51

the resonance sits exactly at threshold.

It renders 19 feature clips and three demo tunes in the firmware step format (3 bytes per step): an original acid line, Bach's Prelude in C and Beethoven's *Ode to Joy*. The audio files are in `docs/audio/features/`.

7 PCB design

7.1 Board and stack-up

The board is 100 mm × 100 mm, 1.6 mm, four layers, with all components on the top side (Table 9). A first two-layer attempt was abandoned:

- it could not be routed completely,
- ground islands between dense traces left pads without a reliable ground,
- some touch lines ran under other keys.

The four-layer stack solves all three problems. It also gives the analog audio path a continuous ground reference, at little extra cost.

Touch pads. On the standard JLCPCB stack-up, the first inner layer lies only about 0.2 mm below the pads. A plane there would dominate the pad capacitance and ruin the touch sensitivity. The pads are therefore protected on the other three layers:

- both inner layers have a copper cut-out under every pad,
- the bottom layer has a pour-free keep-out under every pad, open only in a small strip at the top of the pad where the key's own via and trace arrive,
- on the top layer, the pads have a 1 mm local clearance.

Table 8: Design changes caused by the simulations.

Block	Change	Reason
DCO	2.2 kΩ gate resistor	slower switch-off edge, smaller charge-injection spike
CV filters	10-bit PWM at 46.9 kHz + 2-bit ΣΔ dither	ripple −67 → −81 dB, settling 2.2 → 1.3 ms
CV filters	load-aware networks	correct DC ratios
VCF	ladder capacitors 47 → 33 nF	top of range above 15 kHz
VCF	mixer to VB0 via 10 kΩ / 1 µF, 150 kΩ/470 kΩ sources	settling 0.44 s → 15 ms
VCF	resonance VCA with difference amplifier, 1:13 input, 22 kΩ feedback	no volt-level DC steps into the ladder
VCA	470 kΩ anti-offset resistor	off attenuation 52 → 121 dB
VCA	bases from VREF, 8-bit R-2R trim DAC	feed-through ≈ 100 →< 0.6 mV
VCA	R_E 3 → 4.7 kΩ	maximum gain +11 → +7.4 dB (headroom)
System	audio loopback to PD5	self-test and calibration without extra ICs
Power	VREF follower with 10 Ω + 1 µF snubber	hum −47 → −81 dB, stable

Table 9: Layer stack.

Layer	Use
F.Cu	components, signals, GND pour; no tracks across the keyboard
In1.Cu	solid GND plane
In2.Cu	split power plane: VP under the analog area, +5 V under the MCU column and the keys I/O row, GND under the keyboard
B.Cu	signals, GND pour; below each key only that key's own line

7.2 Floorplan

Figure 16 shows the floorplan:

- **Analog area** (top left): the blocks in signal-flow order, from power and references through the oscillator, ladder, output amplifier and resonance to the VCA and the CV filters.
- **Right-hand column**: MIDI input (not populated), the trim DAC directly next to the VCA, and the MCU.
- **Keys I/O row**: the two multiplexers and the two LED shift registers sit in a full-width row directly above the LEDs and keys. Each chip is above the keys it serves, so the 32 LED and touch lines are short vertical drops instead of long buses across the board.

Moving these chips there from a column on the right made the board routable.

7.3 Placement

Placement is scripted (`hw/pcb_place.py`, `hw/gen_pcb.py`):

- **Anchors**: ICs, the ladder transistor column, connectors, keys and LEDs have explicit positions.
- **Greedy placement**: every other part is placed greedily inside its block, most-connected parts first. Each goes to the free spot that minimises the distance to the pads it connects to, with 0.3 mm spacing to leave routing channels.
- **Decoupling capacitors**: they are placed at their IC's supply pin.
- **Test points**: each goes into the block holding most pins of its net, with its net name printed next to it. VCAOUT and XCUT_IN did not fit and sit on the free top edge.
- **Scope ground**: two through-hole 2.54 mm pins on the top edge.

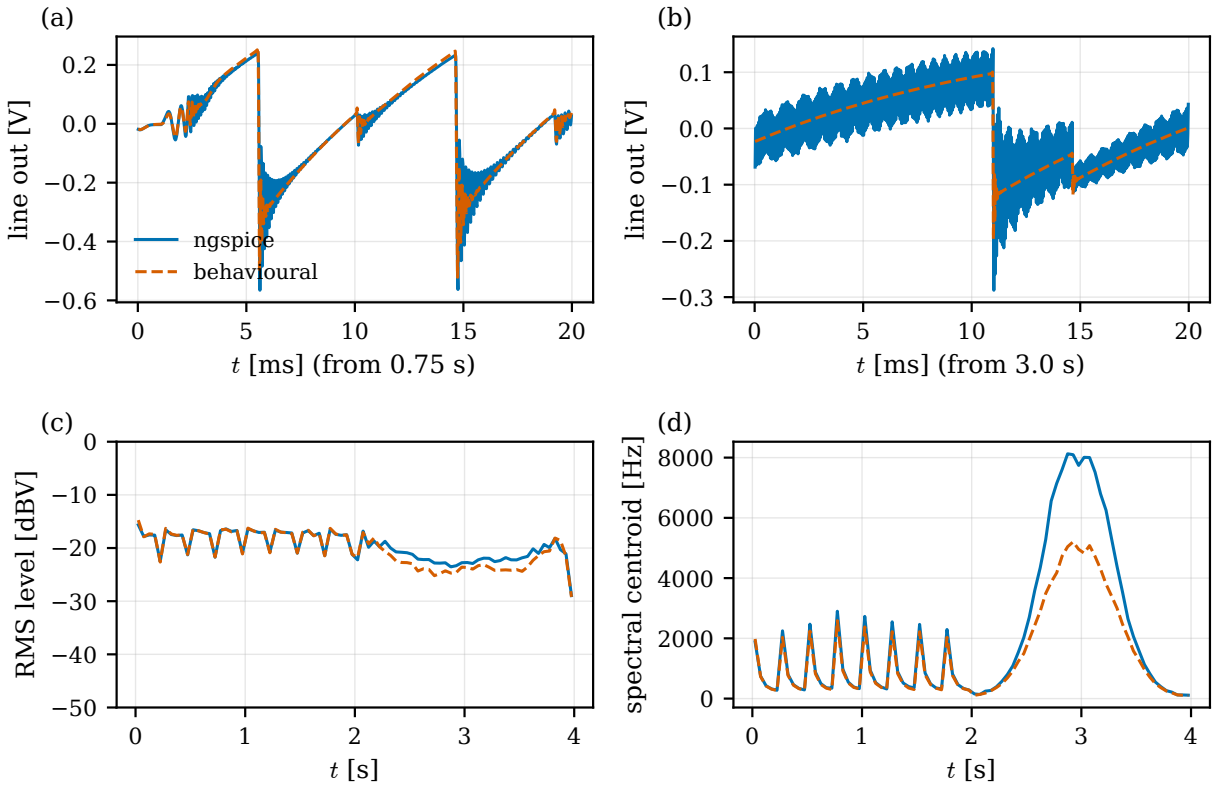


Figure 14: Behavioural model versus ngspice on the S6 score: (a, b) waveform details, (c) RMS level, (d) spectral centroid.

7.4 Routing

Routing is automated in several stages (`gen_pcb.py -route`):

1. **Plane stitching**: every GND, VP and +5 V pad gets a short track to its own via into its plane. The vias are locked so that the autorouter keeps them.
2. **Pre-routing**: the few supply pins outside their plane region are routed on the still empty board with an A* grid router (`hw/pcb_maze.py`) and locked.
3. **Autorouting**: Freerouting 1.9 does two passes. The inner layers are declared as power planes, so signals stay on the outer layers.
4. **Ground grid**: GND stitching vias go on a 2.5 mm grid wherever both outer pours are filled. They keep clear of the mounting holes and of all silkscreen artwork.
5. **Island check**: GND islands are detected by a connectivity analysis and bridged if necessary (`hw/pcb_gnd.py`).
6. **Leftovers**: the A* maze router finishes any remaining connection. A rip-up mode (`-repair`) exists for stubborn cases.

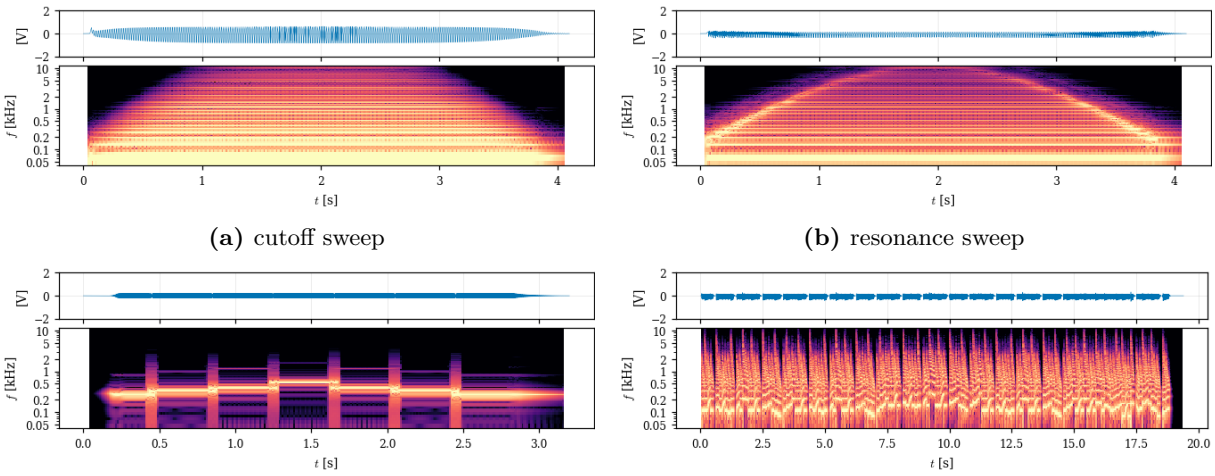
The final board has 0.25 mm tracks (0.3 mm for stitching), 0.2 mm clearance and 0.6 mm/0.3 mm vias, all within JLCPCB's standard capabilities. It has 246 footprints, 1773 track segments (2.5 m on F.Cu, 1.9 m on B.Cu) and 626 vias.

The KiCad design-rule check reports **0 violations, 0 unconnected pads and 0 schematic-parity errors**.

7.5 Silkscreen

The silkscreen documents the design on the board itself:

- a dashed frame with a title for every functional block,
- a piano-style keybed with hatched black keys,



(a) cutoff sweep

(b) resonance sweep

(c) self-oscillation

(d) demo tune (acid line)

Figure 15: Spectrograms of selected behavioural-model clips.

- a strip with the logo, a resonant sawtooth and the ladder response family,
- on the back, the signal-flow diagram and the credits.

All silkscreen text is at least 0.8 mm high with 0.15 mm lines, JLCPCB's minimum.

7.6 Fabrication data

`hw/fab.py` writes the JLCPCB outputs:

- the Gerber files of all four copper layers plus mask, paste, silkscreen and outline, and the Excellon drill file;
- the BOM;
- the placement (CPL) file, with rotation offsets for the SOT, SOIC and TSSOP packages.

The MCU, the headers, the test points, the touch pads and the MIDI parts are excluded from assembly.

8 Bill of materials

JLCPCB assembles 196 parts in 40 BOM lines: 38 Basic and 2 Promotional Extended (BC847BS, CD4051). The components cost about USD 3.65 per board at list price, excluding PCB, assembly fees and the MCU (Table 10). The design has 242 parts in total; 5 are marked do-not-populate (the MCU and the MIDI input).

Table 10: Assembled parts (JLCPCB PCBA, top side). Unit prices from the JLCPCB parts list at the time of design.

Value	Qty	Package	LCSC	Library	USD/pc	Designators
4.7k	29	0603	C23162	Basic	0.0028	R16–R31, R49, R50, R56, R58, R75, R76, R83, R84, R91, R92, R95, R102, R103
10k	17	0603	C25804	Basic	0.0018	R6, R7, R55, R63, R64, R66, R67, R73, R81, R82, R85–R88, R104, R106, R109
1k	15	0603	C21190	Basic	0.0026	R1, R9–R12, R48, R52, R57, R62, R74, R78, R90, R94, R98, R99
100k	10	0603	C25803	Basic	0.0031	R34, R36, R38, R40, R42, R44, R46, R65, R68, R108

Value	Qty	Package	LCSC	Library	USD/pc	Designators
200k	9	0603	C25811	Basic	0.0023	R32, R33, R35, R37, R39, R41, R43, R45, R47
15k	4	0603	C22809	Basic	0.0029	R51, R77, R93, R110
470k	4	0603	C23178	Basic	0.0030	R70–R72, R96
33k	3	0603	C4216	Basic	0.0022	R53, R59, R97
22k	3	0603	C31850	Basic	0.0041	R89, R105, R107
1.5k	2	0603	C22843	Basic	0.0019	R5, R60
2.2k	2	0603	C4190	Basic	0.0018	R8, R54
1M	1	0603	C22935	Basic	0.0019	R100
2M	1	0603	C22976	Basic	0.0025	R101
2.4k	1	0603	C22940	Basic	0.0026	R13
9.1k	1	0603	C23260	Basic	0.0031	R2
10	1	0603	C22859	Basic	0.0032	R3
3.3k	1	0603	C22978	Basic	0.0026	R4
300k	1	0603	C23024	Basic	0.0054	R61
150k	1	0603	C22807	Basic	0.0044	R69
6.2k	1	0603	C4260	Basic	0.0023	R79
120k	1	0603	C25808	Basic	0.0015	R80
100n	17	0603	C14663	Basic	0.0122	C2, C4, C6, C15, C17–C22, C26, C28, C34, C36, C41, C45, C48
33n	8	0603	C21117	Basic	0.0106	C23, C27, C30–C33, C37, C42
1µ	8	0603	C15849	Basic	0.0752	C3, C7–C9, C16, C35, C39, C44
10µ	5	0603	C96446	Basic	0.0541	C1, C10–C13
22n	3	0603	C21122	Basic	0.0083	C24, C38, C43
10µ	3	0603	C19702	Basic	0.0319	C5, C14, C46
1n	2	0603	C1588	Basic	0.0089	C29, C47
10n	1	0603	C57112	Basic	0.0108	C25
4.7µ	1	0603	C19666	Basic	0.0294	C40
red	16	0603	C2286	Basic	0.0075	D3–D18
SS14	1	D	C2480	Basic	0.0191	D1
BC847BS	8	SOT-363	C41375126	Promo	0.0281	Q4–Q9, Q11, Q13
MMBT3904	4	SOT-23	C20526	Basic	0.0115	Q1, Q3, Q10, Q12
2N7002	1	SOT-23	C8545	Basic	0.0178	Q2
TL072	3	SOIC-8	C6961	Basic	0.1613	U2, U10, U11
74HC595	3	SOIC-16	C5947	Basic	0.1152	U7–U9
CD4051B	2	SOIC-16	C21379	Promo	0.2574	U5, U6
78L05	1	SOT-89-3	C71136	Basic	0.0892	U1
LM324	1	SOIC-14	C71035	Basic	0.1658	U12
196 parts		40 BOM lines			3.65	per board (parts only)

Hand-soldered (not in the assembly BOM):

- the MCU (CH32V003F4P6 or CH32V002F4P6),
- the pin headers: power, line out, SWIO, MIDI and the two scope-ground pins,
- optionally the MIDI parts (LTV-817S, 1N4148W, 220 Ω and 470 Ω).

9 Firmware

Firmware version 0.1 (`firmware/touchsynth/`) is built on ch32fun for the CH32V003, CH32V002 and CH32V006 from one code base. With the three demo tunes it uses 14.1 KB of the 16 KB flash of the smallest part. The CH32V006 build (44.4 KB) also holds the multitrack parts of Section 10 and the digital voice on the PWM DAC (Section 10.5). It runs on board 1 (Section 11.3). Its structure follows the timing of the design:

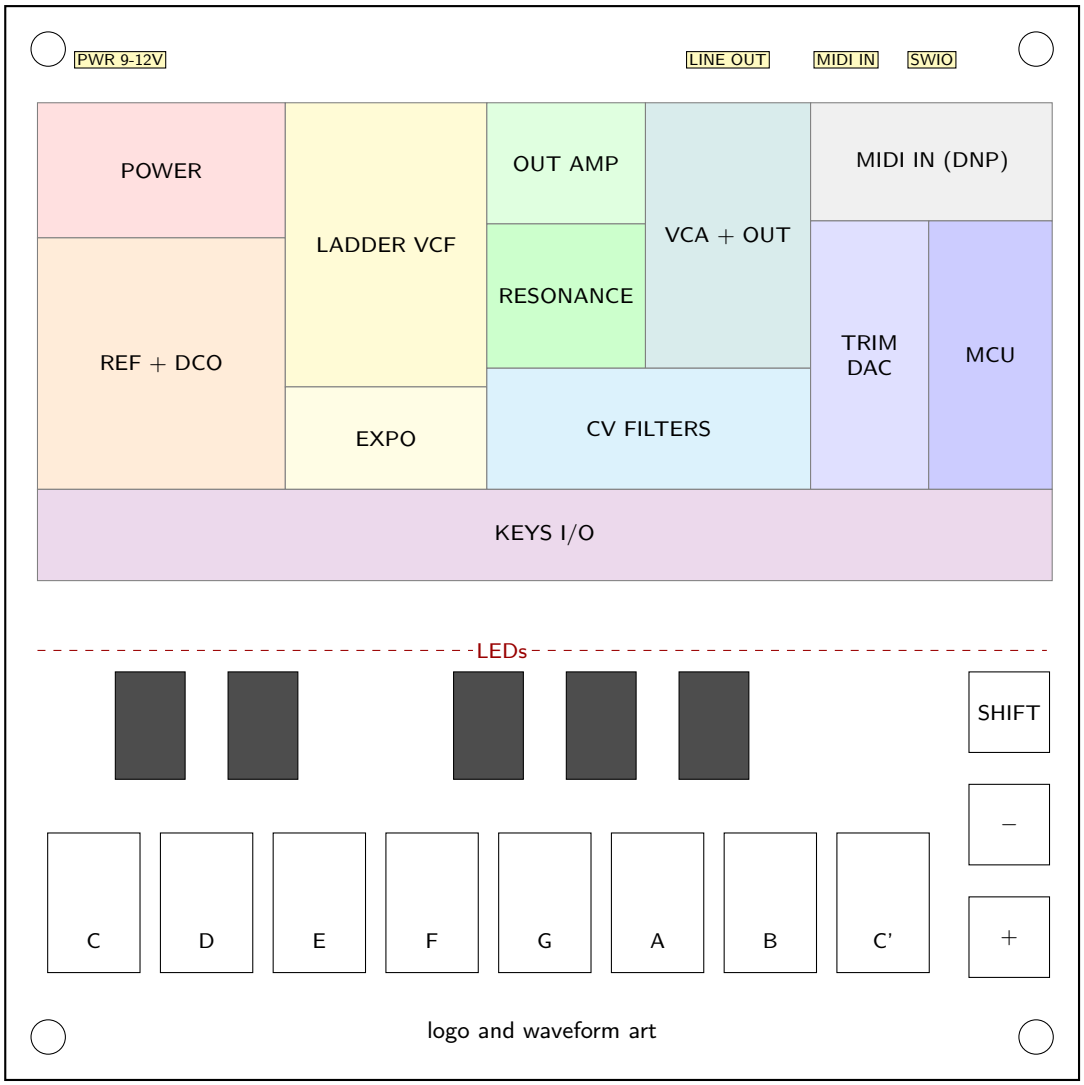
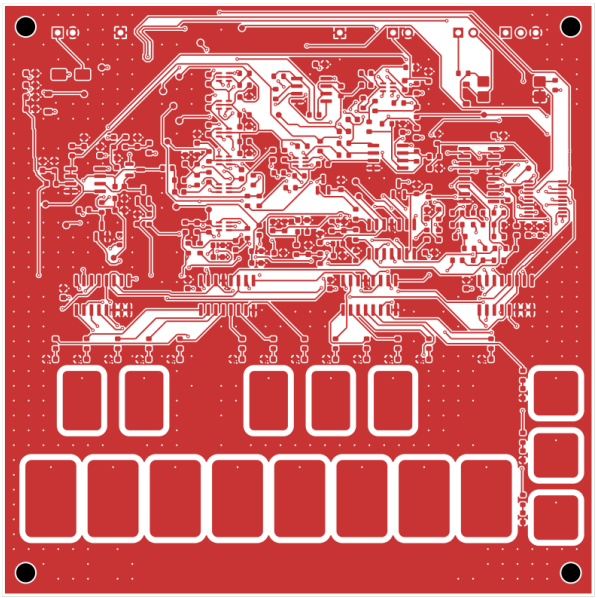


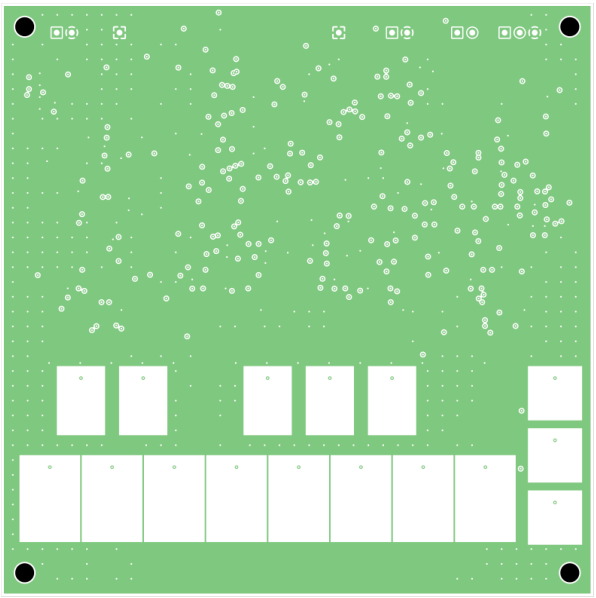
Figure 16: Floorplan (generated from `hw/pcb_place.py`). Connectors along the top edge; the scope ground pins and test points are not shown.

- **TIM1 update interrupt** at 46.875 kHz: loads the four CV compare registers with 2-bit sigma-delta dither (10-bit PWM, 12-bit effective) and clocks the noise LFSR. An interrupt was chosen over DMA bursts for simplicity; it costs a few percent of the CPU.
- **TIM2**: the DCO period. Channel 1 produces the 3 µs active-low reset pulse, channel 2 the pulse wave, and the update interrupt toggles the sub-oscillator. In DAC mode (CH32V006 only) TIM2 instead counts up and down at a fixed 93.75 kHz with the DCO held in reset, and DMA1 channel 2 loads the channel-2 duty from a ring buffer on every update (Section 10.5).
- **Control loop** at 1 kHz (SysTick): glide, LFO, envelopes, key tracking, the CV laws, the percussion pitch envelope and wave switch, and the tune player. It mirrors the firmware layer of the behavioural model. All maths is fixed point, because the CH32V003 has no multiplier.
- **Main loop**: the touch scan of all 16 pads through the multiplexers with per-pad baselines and thresholds, the SHIFT/−/+ user interface, the LED and trim-DAC shift registers, MIDI input, a test console over SWIO for the verification plan (Section 11), and in DAC mode the DSP that refills the DAC ring buffer.

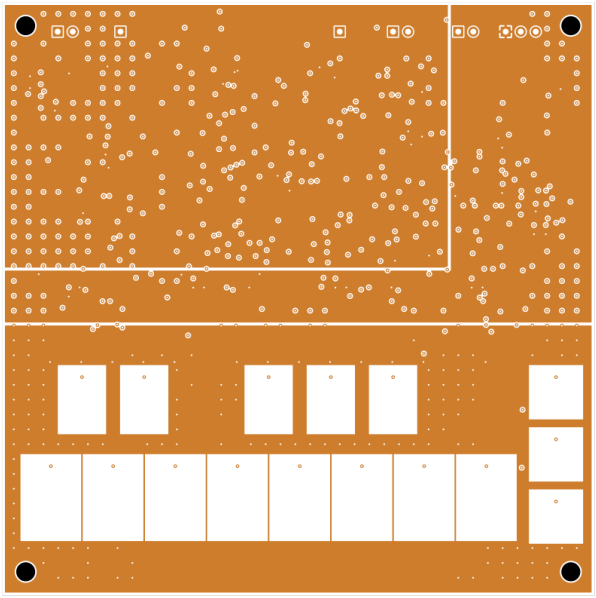
The calibration tables, presets and demo tunes are generated from the simulation results and `tunes.py` by `gen_tables.py`; nothing is copied by hand.



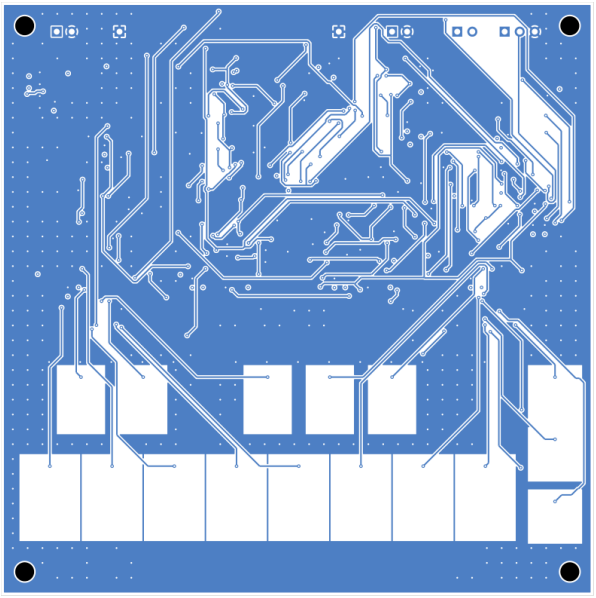
(a) F.Cu



(b) In1.Cu (GND)

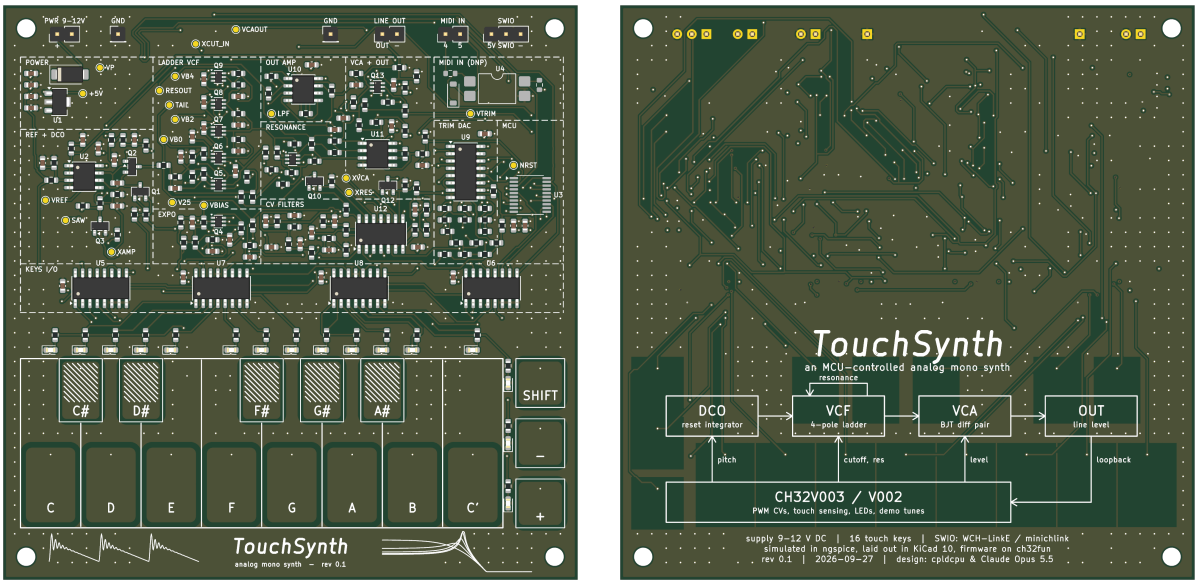


(c) In2.Cu (VP / +5 V / GND)



(d) B.Cu

Figure 17: Copper layers (seen from the top).



(a) top **(b)** bottom

Figure 18: Rendered board.

Pin assignment check. Writing the firmware was also a check of the pin assignment. `check_pins.py` compares every pin constant in the firmware with:

- the net in the design,
- the port in the KiCad symbol,
- the timer, USART and ADC function of that port on each chip family.

All 16 signal pins pass on both families. The check found one difference that the firmware must handle: the timer remap *codes* differ (Table 11). The same remaps also route complementary outputs to PC3, PC4 and PD1 (SWIO). The firmware never enables them.

Table 11: Timer remaps used by the firmware.

Function	CH32V003	CH32V002 / V006
TIM1 CH1–CH4 → PC6, PC7, PC0, PD3	`TIM1_REMAP` = 01	`TIM1_RM` = 0010
TIM2 CH1, CH2 → PC5, PC2	`TIM2_REMAP` = 01	`TIM2_RM` = 010

10 Demo tunes and instruments

10.1 Tune format and player

A tune is a step sequence in flash with three bytes per step: note, length and flags. The length counts steps of a per-tune step time (a sixteenth note for most tunes, a 20 ms grid for the Toccata), so one step holds up to 255 steps. Each tune names a preset. The flags are:

- **slide**: glide into the note without restarting the envelopes;
- **accent**: the preset's accent filter-envelope depth and level;
- **hold** and **tie**: no release at the end of the step, and continue the previous note. Together they split notes longer than 255 steps;
- **sync**: the VCA opens fully for 4 ms, a marker for aligning multitrack recordings.

Steps with a note number of 128 or more are *control steps*. They take no time and set the cutoff (in 1/16 octave), the resonance, the filter-envelope depth, the waveform mask or the volume. A

preceding ramp step sets a glide time for the next cutoff and resonance targets, which the 1 kHz loop interpolates. All filter sweeps in the pieces are such ramps.

The tunes are written in Python (`sim/behav/tunes.py`, `pieces.py`) and converted by `gen_tables.py`. The behavioural model plays the same step data, including the control steps, so every tune can be heard before it is flashed.

10.2 Built-in demos

All builds hold three demos, cycled with SHIFT + C′:

- **acid**: an original acid line (19 s, preset *acid*);
- **prelude**: Bach's Prelude in C (48 s, preset *arp*);
- **ode**: Beethoven's *Ode to Joy* (35 s, preset *lead* with glide and vibrato).

Board 1 recordings of the three demos are in `docs/audio/hw_board1/`.

10.3 Multitrack pieces

The CH32V006 build also holds 30 single-voice parts of four multitrack pieces (Table 12). The synth is monophonic, so a piece is recorded one part at a time from the line out and mixed on the PC:

- **Recording**: the console disables the touch keys (`keys 0`) and starts the part. The oscilloscope records a single shot of 50 M points with 8-bit resolution, which `tools/scope.py` boxcar-decimates to 100 kS/s. The averaging (oversampling) raises the resolution.
- **Alignment**: each part starts with a sync step. If a take was captured without its sync pulse (the scope triggers only after its pre-trigger memory is full), its envelope is cross-correlated with the model render of the same part instead.
- **Clock**: the RC oscillator differs by about 0.1 % between takes. The clock of each take is fitted from its note onsets (residual 2–5 ms rms), and the take is resampled onto a common clock.
- **Mix** (`tools/mix_parts.py`, `suite.py`): noise gate, pan, Haas widening on pads, ping-pong delay and convolution reverb.

Table 12: Multitrack pieces. Audio in `docs/audio/demo/` and `docs/audio/pieces/` (`_hw`: board 1, `_model`: behavioural model).

Piece	Source	Parts (preset)	Length
TouchSynth Demo	original, 118 bpm, 69 bars	kick, snare, hat, bass (acid), arp, lead, pad (sweep)	2:24
Queen Mary's March	Purcell, Z 860, WIMA edition for four trumpets; two passes with filter sweeps	4 trumpets (brass), 16′ bass (pedal), timpani (kettle, PWM DAC)	2:41
Toccata, mm. 1–30	Bach, BWV 565, MusicXML; mordents and trill written out, fermatas doubled	8 manual tracks (organ), pedal	2:02
Aerosphere	original, in the style of 1970s space-synth music, 100 bpm, 68 bars	wind, 2 pads (strings), sequence (seq), bass (pedal), lead (theremin), kick, hat	2:53
Suite	Aerosphere intro (wind, pads) dissolving into the Toccata	–	2:19

The Toccata has up to nine simultaneous voices. They are allocated to the eight manual tracks by nearest pitch, so each track plays a continuous line and no note is dropped. Purcell's score has no drum part; the timpani on C and G (tonic and dominant) are an addition and follow the harmony bar by bar.

10.4 Instruments

Every instrument is a preset of the one voice (Table 13): the waveform mask (saw, pulse, sub-octave square, noise), cutoff with key tracking, filter-envelope depth, resonance (1 = self-oscillation threshold), two ADSR envelopes, glide and an LFO on pitch or pulse width.

- **Brass**: saw and pulse with a slow filter attack (60 ms), so each note opens from dark like a trumpet.
- **Organ, pedal**: organ is saw, pulse and sub with full sustain and fast attack and release. Pedal is a saw without the sub: on board 1 the sub-octave of low pedal notes (33 Hz) was heard as pumping.
- **Strings**: a slow pulse-width modulation (0.4 Hz) stands in for an ensemble, with slow attack and release.
- **Wind**: noise through the filter just below self-oscillation. Control-step ramps sweep it into pitched gusts.
- **Theremin**: a pulse wave with 120 ms glide and 5.5 Hz vibrato of 25 cent.
- **Seq, acid, arp, lead, sweep**: classic subtractive patches; fast filter envelopes for the sequence and acid line, a slow filter swell for the pad.

Table 13: Presets (`sim/behav/tunes.py`). Cutoff at C4, envelope depth in octaves, ADSR times in s; →: waveform after the wave switch.

Preset	Waveforms	Cutoff [Hz]	Key tr.	Env.	Res.	Filter ADSR	Amp ADSR
acid	saw	170	0.3	3.2	0.80	.002/.09/0/.04	.002/.2/.7/.02
arp	saw + pulse, PWM	700	0.5	3.0	0.55	.001/.12/.1/.1	.002/.18/.4/.12
lead	saw + sub, vibrato	1400	0.6	1.5	0.35	.01/.5/.4/.3	.01/.4/.85/.25
sweep	saw + sub	180	0.3	4.2	0.70	1.6/2.5/.25/1.2	.25/1/.9/1.5
brass	saw + pulse	500	0.6	2.8	0.30	.06/.8/.35/.5	.035/.4/.85/.5
organ	saw + pulse + sub	1800	0.7	1.0	0.25	.005/.3/.6/.2	.005/.2/1/.15
pedal	saw	300	0.3	1.5	0.30	.01/.5/.4/.6	.01/.3/1/.6
strings	saw + pulse, PWM	900	0.5	1.0	0.20	.8/1.5/.6/1.5	.6/1/.9/1.5
wind	noise	300	0	0	0.90	–	1.5/1/1/3
seq	saw + pulse	400	0.5	3.0	0.60	.001/.12/0/.1	.001/.2/.3/.12
theremin	pulse, glide, vibrato	1200	0.6	0.5	0.20	.2/.5/.8/.6	.15/.5/.9/.6
kick	sub + noise → sub (3 ms)	300	1.0	2.0	0.15	.001/.012/0/.03	.001/.2/0/.06
snare	pulse + noise → noise (20 ms)	2600	0	1.3	0.15	.001/.06/0/.04	.001/.12/0/.05
hat	noise	8500	0	0.5	0.55	.001/.015/0/.02	.001/.018/0/.02
timpani	all four → saw + pulse (40 ms)	262	1.0	0	0.88	–	.004/.45/0/.4
kettle	PWM DAC: 17 modal resonators	4000	0	0	0	–	.001/5/1/2

Percussion. The voice has no drum circuits, so percussion comes from the firmware. Version 3 of the drum presets, recorded on board 1, did not sound like drums:

- the kick was a sub square at a constant 41 Hz, with no pitch drop and no attack;
- the snare's 146 Hz tone rang as long as its noise, because tone and noise share one filter and one VCA;
- the tom was a resonant filter ring sliding down from about 720 Hz.

Version 4 adds three engine functions, the same in the firmware and the model:

- **Pitch envelope**: the DCO is a timer, so the 1 kHz loop can retune it every millisecond. A preset gives an offset in semitones at the attack, which decays exponentially to the note. Key tracking follows, so the filter moves with the pitch.
- **Wave switch**: a set time after each attack the waveform mask changes. This separates a drum's tone and noise in time, although they share the filter and the VCA.
- **Source muting**: while the amplitude envelope is below −66 dB, all sources are off. Otherwise they leak through the closed VCA at about −40 dB in drum tails and rests.

With these the kick falls from 220 Hz to its 55 Hz body within about 80 ms, behind a 3 ms noise click (Figure 19a). The snare has a pulse body falling a fifth for 20 ms, then only bright noise. The hat uses a high, resonant cutoff and reaches −20 dB after 37 ms (previously 75 ms).

The first, analog timpani preset was matched to a recorded timpani: the resonance peak is locked onto the second harmonic by key tracking (the peak lies at about 2.1 times the cutoff value), the pulse wave partly cancels the saw fundamental, and for the first 40 ms the sub-octave square and noise add attack partials. It rests on a misreading of the recording by one octave (see below): its strongest partial sits an octave above the note. One periodic oscillator cannot produce a drum's inharmonic modes in any case; the kettle of Section 10.5 supersedes it.

On board 1 the version 4 drums behave as in the model. The kick peaks after 2.6 ms (version 3: 20 ms) and falls from 108 Hz in the first 10 . . . 30 ms to 55 Hz. The snare's noise centroid is 3.1 kHz at 30 . . . 80 ms (version 3: 0.9 kHz), and the snare reaches −20 dB after 102 ms (317 ms). The hat reaches −20 dB after 41 ms. The analog timpani's partials on the board match the model within a few dB: over 40 strokes on C3 and G2 the fundamental is at −11 dB and the third harmonic at −36 dB relative to the second, so the resonance peak lands on the second harmonic. The kick's body decays more slowly on the board than in the model (−20 dB after about 0.4 s).

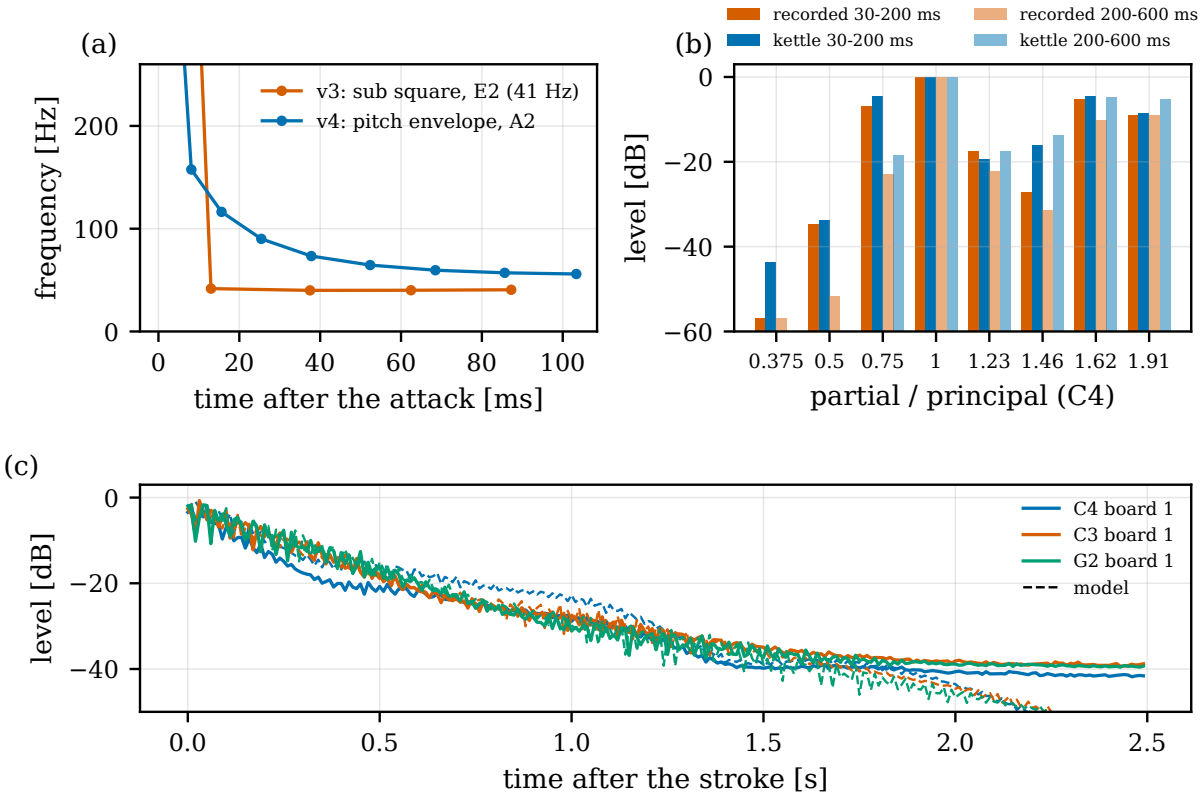


Figure 19: Percussion (`tools/instrument_figures.py`). (a) Kick pitch after the attack in the behavioural model: version 3 (constant sub square) and version 4 (pitch envelope). (b) Kettle partials in two time windows, relative to the principal: a recorded timpani (C4 stroke) and the kettle preset at C4 in the model. (c) Kettle decay on board 1 (solid) and in the model (dashed) for C4, C3 and G2; below about −40 dB the board's noise floor takes over (`docs/results/hw_board1_kettle.csv`).

10.5 Kettle: a modal timpani on the PWM DAC

A drum's sound comes from the modes of its membrane: inharmonic partials, each with its own decay. The analog voice has one periodic oscillator and one filter, so it cannot produce them. Modal synthesis can: a bank of resonators, one per mode, excited by the strike. That needs an audio DAC, and the pulse output can serve as one without any hardware change.

Pulse output as PWM DAC. In DAC mode TIM2 counts up and down over 2 × 256 ticks, a 93.75 kHz carrier with 8-bit duty and pulses centred in the period. Centred pulses keep the signal from also modulating the pulse position, which with simple up-counting PWM added a second harmonic of 0.6 % (S8). DMA1 channel 2 loads the channel-2 duty from a ring buffer on every timer update. In this mode the update comes at both ends of the period, so each period's duty is stored twice, and the CPU only fills the buffer. The DSP produces samples at 15.625 kHz and interpolates linearly from one sample to the next over the 6 carrier periods of a sample, which lowers the sampling images by about 23 dB. Each period's duty is quantised with first-order error feedback, which shapes the quantisation noise towards the carrier, so the 8-bit DAC reaches about 10–11 bits in the audio band. The pulse pin feeds the passive mixer (470 kΩ into 10 kΩ, then 1 µF) and the ladder, which acts as the reconstruction filter. The ladder's input pair sees only the two PWM levels, so its tanh characteristic does not distort the duty-cycle code. S8 (Section 5.9) checks the path in ngspice. Filter, resonance and VCA keep working on the digital signal. The analog oscillator is parked in reset meanwhile, so a preset is either analog or digital.

Modal synthesis. Each stroke excites a bank of two-pole resonators, one per mode:

$$y[n] = 2r\cos\omega\; y[n-1] - r^2\, y[n-2] + b\, x[n],$$

with ω from the mode's frequency, $r = e^{-1/(\tau f_s)}$ from its decay time τ and $b = a\sin\omega$ for its level a. The excitation x is a raised-cosine mallet pulse of 1 ms (a hard mallet; a shorter contact excites the upper modes more). There are two banks, so two drums can ring at once. A stroke on a note that is still ringing adds to its bank, as on a restruck drum; a new note takes a free or the oldest bank. The sum passes a cubic soft clipper ($1.5x - 0.5x^3$) before the encoder: rolls on a ringing drum add up, and the clipper rounds the rare peaks instead of cutting them.

Fit to a recorded timpani. The modes were fitted to a recorded F3–A3–C4 triad. In each stroke the principal mode at the note carries the pitch. A mode at 0.75 times the note leads the first 30 ms and fades within about 0.1 s, and a short thud lies at 0.375 times. Modes at 1.23, 1.46, 1.62 and 1.91 times colour the tone; the F and C strokes show the same ratios. The first fit read the strong 262 Hz partial of the C stroke as the octave of a C3 drum, which put every mode an octave too high. The identical ratios in the F stroke resolved it.

The preset is deliberately harder and more metallic than the recording:

- the 1 ms mallet;
- the upper modes louder than in the recording, but still below the principal and decaying no slower, so the pitch stays on the note;
- four more high modes between 2.2 and 3.3 times the note;
- each strong mode doubled 0.4 % higher, 3 . . . 8 dB weaker. A real membrane's modes are split into such pairs, and their beating gives the shimmer.

That makes 17 resonators. Figure 19b compares the partials with the recording.

Firmware. Signals are fixed point (Q24) with Q30 coefficients and use the CH32V006's hardware multiplier; the coefficients are computed in floating point once per stroke. The main loop refills 128-sample halves of the ring, 8.2 ms each. The CH32V003 and V002 have no multiplier or too little RAM and keep the analog voice only. Four problems appeared on board 1:

- **Stack overflow.** With the DSP state and the ring buffer, only 280 bytes of the 8 KB RAM were left for the stack, which overwrote the patch and the CV values. The ring now shares the console's 4 KB capture buffer (captures are refused in DAC mode); 1.4 KB remain.
- **Stalled control tick.** Selecting the kettle blocked interrupts for over 1 ms. The SysTick handler schedules the next tick by adding to the compare value, which then lay in the past,

so the next match came only after a counter wrap and the 1 kHz engine stopped. The handler now resynchronises when it falls behind, and the soft-float set-up no longer runs with interrupts blocked.
- **DSP too slow.** At first a refill took the whole half. The DSP rate was halved to 15.625 kHz (the highest kettle mode is below 1 kHz; the 4 kHz cutoff suppresses the sampling images). The excitation term is computed only during the mallet contact, and the refill loop runs from SRAM instead of flash. A refill now takes at most 4.7 ms of the 8.2 ms half.
- **Blocking console wait.** The console's `wait` command blocked the main loop and starved the DAC during test sequences; it now keeps the DAC fed.

The console command `dac` reports the DMA position, late refills and the longest refill.

Board 1 results.
- **DMA:** the transfer counter advances by 19 in 100 µs, two updates per 93.75 kHz period, so the TIM2 update request is served by DMA1 channel 2 as assumed, and the pitch is the same as with the first, edge-aligned version.
- **Centred pulses and interpolation:** against the first version (edge-aligned PWM, samples held) the share of 8 to 20 kHz in a C3 stroke drops from −38 to −43.5 dB, and the noise in a decaying tail from 2.6 to 2.2 mV rms.
- **Pitch:** C4, C3 and G2 strokes sound at 259.6, 129.9 and 97.3 Hz: the note scaled by the board's −0.8 % clock, like every other pitch. In the recorded March part, 13 of 13 G2 strokes and 26 of 27 C3 strokes have their strongest partial on the note.
- **Decay:** within 1 . . . 4 dB of the model down to about −40 dB, where the board's noise floor takes over (Figure 19c).
- **Timing:** no late refill in the test sequence, and the March take fits the common clock with 3.3 ms rms, so the DSP kept up through the whole part.
- **Open:** a faint line at 122 Hz, the buffer-half rate, 61 dB below the take's peak. It is at the level of the board's noise floor and probably comes from the DSP's current bursts reaching the analog supply.
- **Carrier crosstalk:** the 93.75 kHz carrier reaches the line out at about 5.8 mV rms, far more than the filter path lets through (S8). Closing the VCA hardly changes it (4.9 mV), so it couples past the filter and the VCA, presumably from the PWM pin on the board. It is ultrasonic: in the audio band the line out stays at the board's noise floor (0.32 mV at 2 to 8 kHz, measured at 1 MSa/s). But a long scope take is sampled at only 200 kSa/s (50 Mpts for 200 s), which folds the carrier's sidebands into the audio band; the board recordings therefore show about twice the true noise at 2 to 8 kHz. A passive low-pass in front of the scope, or an audio interface, avoids that. A higher carrier would fold outside the audio band, but needs a faster DMA refill than the main loop allows.
- **Console traffic:** each console exchange blocks the main loop for about 20 ms, longer than a buffer half; the recorder therefore no longer polls the console during a take.

The March recorded on board 1 uses the kettle (`docs/audio/pieces/march_hw.mp3`). In the same folder, `kettle_model.mp3` plays the triad and the March pattern in the model.

11 Verification and validation plan

Verification is organised in five levels (Table 14). Levels L2 and L3 are designed to run automatically. A host script drives the test firmware over the WCH-LinkE debug interface with `minichlink`. It captures the audio loopback, computes spectra and compares them with limits derived from the simulations. The results are stored as CSV next to the simulation data, so hardware and simulation can be plotted together.

Table 14: Verification levels.

Level	Content	Method
L0	design verification	ngspice S1–S7 (done)
L1	assembly and bring-up	DMM on the test points, current-limited supply
L2	functional tests T1–T14	test firmware + loopback ADC via `minichlink` (automated)
L3	calibration	per-board constants stored in flash (automated)
L4	validation	playing, listening, long-run stability (user)

11.1 Bring-up

Bring-up starts with the MCU not fitted, using a lab supply at 9.0 V with a 100 mA current limit and the multimeter ground on one of the two scope-ground pins. The expected values in Table 15 are the DC operating point of the simulation netlist in exactly this state (`sim/bringup/bringup_op.py`, results in `docs/results/bringup_expected.csv`). Without the MCU its pins float:

- **Linear CVs at zero**: the AMP, RES and VCA filter networks are pulled to 0 V by their 15 kΩ last-stage resistor, so resonance is off and the VCA is shut.
- **Cutoff CV at VBIAS**: the cutoff network has no DC path of its own. XCUT_IN floats up to VBIAS through the expo divider, both expo bases sit at VBIAS, and the ladder tail carries the expo reference current (about 8 µA). Once the MCU drives the pin low, XCUT_IN drops to about 0.2 V and the tail current to nearly zero.
- **DCO held in reset**: the reset level shifter has no base drive, so the 2N7002 shorts the integrator capacitor and SAW sits at VREF.
- **Random shift-register state**: the 74HC595s power up with random outputs. Any number of the 16 red LEDs (about 0.68 mA each) may light, which moves the input current between the two values given for B3, and VTRIM can be anywhere between 0.4 and 5 V.

The ladder bias taps are a divider from VP, so B7 is judged as the ratio to the measured VP. The other limits leave room for resistor (1 %) and reference tolerances. A value outside its limit points to the block on that test point's silkscreen frame.

Board 1 result (MCU not fitted). B1–B10 pass. All three 74HC595s came up with every output high (16 LEDs lit, VTRIM at code 255), which is a legitimate power-up state. Two observations:

- **VP** is 0.15 V below the simulation: the SS14 drops about 0.43 V at 25 mA instead of the model's 0.28 V (or the supply leads drop part of it). The ratiometric parts of the design do not depend on it.
- **Ladder bias**: relative to VP, VB0 is 0.9 % low and VB2 / VB4 are about 1.7 % low. That is inside the limit but more than the resistor tolerance alone explains: roughly 50 µA leaves the chain at the upper taps. TAIL follows VB0 minus one V_{BE} and is consistent with it. To be watched in the VCF tests (T6–T8).

The first bring-up also corrected two simulation models: the 78L05 model drew only its quiescent current from the input, and the TL072 macromodel drew about 4 mA per amplifier instead of the datasheet 1.4 mA. Both are fixed in `sim/models/models.lib`. With them, the simulated input current with all LEDs lit is 25.7 mA, against 25 mA measured. The first version of Table 15 had also driven the PWM nodes to 0 V; that is the MCU-fitted state, not the floating one, and gave wrong expectations for XCUT_IN, TAIL and VBIAS.

After B11 the firmware drives the LEDs (octave display), sets the trim DAC to mid-scale (VTRIM about 2.7 V, loaded by the 1 MΩ injection resistor) and drives the cutoff PWM low (XCUT_IN about 0.2 V). With `cv vca 0` and no note playing, B9–B10 should still hold.

Table 15: Bring-up steps, MCU not fitted except B11–B12 (lab supply, current limit 100 mA). Expected values from the DC operating point of the netlist; board 1 measured at 9 V, 2026-10-17, all 16 LEDs lit.

#	Step / test point	9 V in	12 V in	Limit (9 V)	Board 1
B1	visual check; unpowered: no short VP, +5V to GND	–	–	–	–
B2	reverse polarity, 1 s	$I < 1$ mA	–	pass	0 mA
B3	input current	14.8 / 25.7 mA[a]	15.9 / 26.8 mA[a]	10 … 35 mA	25 mA[a]
B4	VP	8.72 V	11.72 V	8.4 … 8.9 V	8.57 V
B5	+5V	5.00 V	5.00 V	4.8 … 5.2 V	5.028 V
B6	VREF	4.50 V	4.50 V	4.45 … 4.55 V	4.53 V
B6a	VBIAS / V25	1.56 / 2.50 V	1.56 / 2.50 V	±3 %	1.57 / 2.515 V
B7	VB0 / VB2 / VB4	2.46 / 4.48 / 6.50 V	3.28 / 6.00 / 8.72 V		2.39 / 4.32 / 6.28 V
	as ratio to VP	0.281 / 0.513 / 0.745		±3 %	0.279 / 0.504 / 0.733
B8	TAIL	1.96 V	2.79 V	1.8 … 2.1 V	1.88 V
B9	LPF	4.50 V	4.50 V	4.3 … 4.7 V	4.53 V
B10	SAW / RESOUT / VCAOUT	4.50 V	4.50 V	4.3 … 4.7 V	4.52 / 4.52 / 4.51 V
B10a	XAMP / XRES / XVCA	0 V	0 V	< 50 mV	0 / 0 / 0 V
B10b	XCUT_IN	1.56 V	1.56 V	±3 %	1.57 V
B10c	VTRIM	0.4 … 4.96 V[b]	0.4 … 4.96 V[b]	–	4.92 V[b]
B11	MCU fitted, `id`	–	–	answers	pass[d]
B12	current, MCU on	20 … 31 mA[c]	21 … 32 mA[c]	< 40 mA	25 mA[e]

[a] all LEDs off / all 16 LEDs on (random 74HC595 state at power-up); board 1: all on. [b] random 74HC595 state; 4.96 V = code 255. [c] MCU ≈ 5 mA, 1 to 16 LEDs lit. [d] CH32V006, firmware 0.1, reply `touchsynth 0.1 CH32V006`. [e] firmware idle, all LEDs off; 12 V not recorded.

Board 1 result (MCU fitted). Board 1 carries a CH32V006. It was flashed with firmware 0.1 through a WCH-LinkE and `minichlink` on a Linux host, which also carries the text console over SWIO (`tools/synthtest.py`). B11 and B12 pass. The input current of 25 mA with the firmware idle and all LEDs off is about 5 mA above the expected 20 mA, which suggests that the MCU draws about 10 mA rather than the assumed 5 mA; it is well inside the limit. Bring-up found one board defect and several firmware faults, all fixed:

- **PD4/PD5 solder bridge** (MCU pins 1 and 2, hand-soldered TSSOP). The loopback input read 0 V instead of about 2.7 V: 4.5 V on the VCAOUT side of R109 and 5 mV on the ADC side. Two console diagnostics located it: `adc <ch>` reads any ADC channel, and `latch <0|1>` holds the 74HC595 latch line (PD4) and reads port D back. With the latch line high, PD5 read 4089 counts like PD4. After rework the loopback sits at 2209 counts (VCAOUT 4.52 V).
- **Trim DAC MSB lost.** SRCLK of the LED/DAC shift-register chain is shared with mux select S1. A touch scan ended with it high, so the first rising edge was missing and the first bit shifted out, the DAC MSB, was lost. `hw_leds_dac` now pulls the clock low before the first bit (found in T1).
- **Loopback ADC on the V00x.** The ADC has to be re-armed before every conversion; without it the capture hung. The sample time was also shortened so that 5 µs captures keep up, and the capture buffer holds 2048 samples on the V006.
- **Touch calibration.** The first noise estimate underflowed in unsigned arithmetic and gave some pads unreachable thresholds; it is now a signed deviation statistic over 64 scans. Pad 0 reads about 550 counts low right after reset, which held key C on; a 300 ms warm-up scan precedes the calibration. During long recording sessions ghost touches still occurred, because the noise estimate came out as low as 48–96 counts on some boots. A threshold floor (`TOUCH_MIN_THR` = 200 counts, against at least 486 counts for a real touch) and a two-scan debounce removed them.
- **Function-pad LEDs.** The LEDs next to SHIFT, − and + were never lit in normal playing:

by design, the firmware used them only in edit mode or as the top of a value bar. The hardware was confirmed with `leds 0xe000`, after fixing the console's hex parser. The LEDs now light while their pad is touched.

11.2 Functional tests

Table 16: Functional tests (board 1: run from the PC with `tools/hwtest.py` over the console), limits derived from the simulations.

ID	Block	Procedure	Pass limit (sim)
T1	LEDs, 595 chain	walking one; trim DAC walk shifts VCAOUT DC monotonically	monotonic, $>$ 20 mV span
T2	touch	256 readings per pad untouched; user touches each pad	$\sigma < 2$ LSB (V003) / 6 LSB (V002); $\Delta > 10\sigma$
T3	touch scan	time a full 16-pad scan	$\geq$ 200 Hz (sim 1.4 kHz)
T4	DCO pitch	loopback capture at C2, C4, C6	$<$ 1 cent
T5	DCO amplitude	loopback amplitude C1–C8	$\pm$5 % after calibration
T6	VCF self-osc. threshold	ramp CV_{RES}, detect sustained oscillation	2.7 … 3.5 V (sim 3.1 V)
T7	VCF tracking	self-oscillation frequency at CV_{CUT} = 1–4.5 V	2.05 $\pm$ 0.2 oct/V
T8	VCF low-pass	110 Hz saw, cutoff 1 kHz, harmonic 10 vs. 1	$\pm$3 dB of sim
T9	VCA gain law	1 kHz saw, CV_{VCA} sweep	max. gain $\pm$2 dB of sim (+7.4 dB)
T10	VCA thump	CV_{VCA} steps without signal, before/after calibration	$<$ 3 mV after (sim 0.6 mV)
T11	CV settling	VCA step seen at the loopback	1 % in $<$ 2.5 ms (sim 1.3 ms)
T12	hum and noise	VCA open, DCO off, spectrum	100 Hz $<$ sim + 6 dB; broadband $<$ $-$60 dB
T14	MIDI (if fitted)	note on/off, pitch bend, CC from a keyboard	all received

11.3 Board 1 functional test results

The functional tests on board 1 (2026-10-17, 9 V lab supply, room temperature) were run from the PC with `tools/hwtest.py`. The script sends console commands (`cv`, `dco`, `trim`, `cap`, `capcv`) and evaluates the loopback captures; the on-chip `selftest` is not implemented yet. The loopback ADC is 12-bit at PD5, which sees 0.6$\times$ VCAOUT and is referenced to +5V (5.028 V): one count is 2.05 mV at VCAOUT. Captures have 2048 samples at 5 … 100 µs per sample. All analog tests use the calibrated trim code 104. Evaluated data are in `docs/results/hw_board1_*.csv`, the raw captures and console logs in `docs/results/hw_board1/`, and Figures 20–23 are generated by `tools/hw_figures.py`. Table 17 summarises the results. All executed tests pass, with two notes: the broadband noise is marginal and the VCA has a slow tail when it opens. T3 and T14 were not run.

Findings.

- **Oscillator and clock.** Pitch and saw amplitude are within limits without calibration (Figure 20); the amplitude spread (-0.9 / $+1.2$ %) is similar to S1. Because the capture is

Table 17: Board 1 functional test results (2026-10-17). Levels in dB are relative to 1.33 V_{pp}.

ID	Board 1 result	Limit (sim)	Verdict
T1	all 16 LEDs light; trim walk 0–255 moves the VCA-open level at VCAOUT monotonically over 366 mV	monotonic, > 20 mV	pass
T2	untouched σ 20–28 counts (pads C–G) and 35–43 counts (G#–+); touches 486–4233 counts, 20–90 σ; no ghost touch in a 180 s log[a]	$\Delta > 10\sigma$	pass
T3	not recorded	$\geq$ 200 Hz	–
T4	−0.28 … +0.26 cent at 11 notes C2–C7, relative to the MCU clock[b]	< 1 cent	pass
T5	saw 1.495 V_{pp} at VCAOUT, −0.9 / +1.2 % over C2–C7, uncalibrated	±5 %	pass
T6	onset between 3.05 and 3.17 V (cutoff code 2211), oscillation at 2.0 kHz	2.7 … 3.5 V (3.1 V)	pass
T7	2.01 oct/V over CV_{CUT} = 0.49–4.02 V (89 Hz – 12.1 kHz), ≤ 45 cent from a straight line	2.05 ± 0.2 oct/V	pass
T8	harmonic 10 at −3.7 dB re harmonic 1; 4-pole fit f_p = 2077 Hz	±3 dB of sim[c]	pass
T9	gain law within −0.23 … +0.05 dB of S4 for CV_{VCA} = 0.25–5 V; off ≥ 81 dB (measurement floor)[d]	±2 dB	pass
T10	thump at VCAOUT −33 mV at trim 128 (default), 0 ± 2 mV at trim 104	< 3 mV after cal.	pass
T11	closing step: 1 % in 1.17 ms; opening step: about 2 % left after 1.5 ms, 1 % after 12.8 ms	1 % in < 2.5 ms (1.3 ms)	pass[e]
T12	50 Hz: −82 dB, 100 Hz: −79 dB; broadband (20 … 5000 Hz) −54 dB with the VCA open, −55 dB closed	100 Hz < −75 dB; broadband < −60 dB	hum pass, noise marginal
T14	not tested	all received	–

[a] A raw reading is the sum of 12 conversions, so the per-conversion σ limit was not evaluated; ghost touches seen later in long sessions led to the threshold floor (Section 11, bring-up). [b] DCO timer and capture share the HSI clock; the absolute pitch is 14 cent flat (see text). [c] an ideal 4-pole low-pass with the S3 cutoff for this code (1.0 kHz at −3 dB) gives −3.5 dB at 1.1 kHz. [d] relative to full gain; the absolute maximum gain (S4: 7.4 dB) was not measured separately. [e] for the CV network (closing step); the opening step has an additional slow component (see text).

timed by the same clock as the DCO, T4 checks the timer arithmetic but not the absolute pitch. From the scope recordings of the demo tunes (232 kick hits against the scope timebase), the HSI runs at 47.62 MHz, −0.80 %. All pitches are therefore about 14 cent flat and the tunes 0.8 % slow until a clock trim is calibrated. Takes recorded up to an hour apart differed by up to 0.1 %, the drift of the RC oscillator.

- **Filter.** Tracking, threshold and slope agree with S3 (Figure 21). At CV_{CUT} = 2.55 V the filter self-oscillates at 1611 Hz; S3 gives 1606 Hz at 2.5 V, so board 1 is about 0.1 octave lower at equal CV, which the cutoff calibration absorbs. The lowest sustained oscillation is 89 Hz at 0.49 V; at 0 and 0.24 V only 5 and 15 mV_{rms} remain. The harmonics scatter by about ±2 dB around the 4-pole fit, and the fitted pole frequency (2077 Hz) agrees with the self-oscillation frequency at the same code (about 2.0 kHz, T6). The low ladder bias seen in B7 has no visible effect.
- **VCA.** The gain law follows S4 within 0.25 dB (Figure 22). The thump is linear in the trim code (−1.4 mV per code) and nulls at code 104, inside the expected 30–230. The firmware still boots with code 128, which leaves −33 mV, until the calibration store exists. The closing step settles to 1 % in 1.17 ms (S2: 1.3 ms). The opening step reaches about 2 % in 1.5 ms and creeps in over another 10 … 15 ms. A linear RC network would settle alike in both directions, so the tail is most likely thermal: the VCA transistors warm up when their current jumps from zero. One ADC count is 0.9 % of this step, so the tail is resolved only coarsely. At note-on it is a level creep of about 2 %.
- **Hum and noise.** The 100 Hz hum (−79 dB) is at the noise floor with the lab supply; a test with mains adapters (V6) is still open. The broadband floor up to 5 kHz is about −55 dB (total 1.19 … 1.29 mV_{rms} at VCAOUT with the discrete lines included, about −52 dB). It is nearly the same with the VCA closed, and the quantisation of the loopback alone (0.59 mV_{rms}) corresponds to −58 dB, so the loopback cannot verify the −60 dB goal. The scope recordings

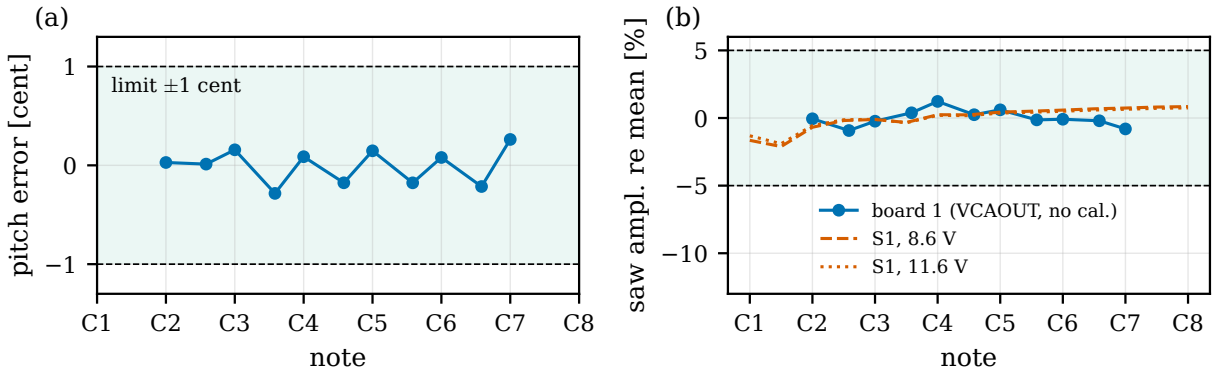


Figure 20: Board 1, T4/T5: (a) DCO pitch error from the loopback capture, relative to the MCU clock; (b) saw amplitude at VCAOUT relative to its mean, without calibration, next to the S1 amplitude at both supply corners.

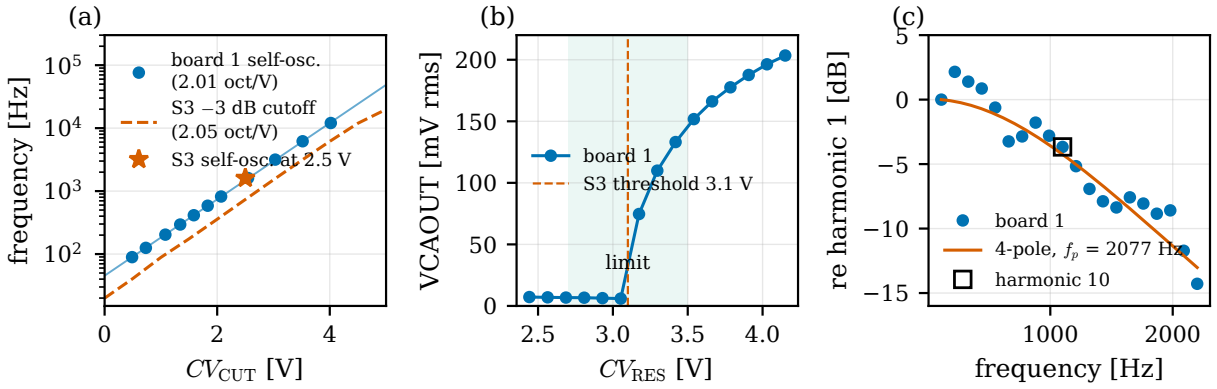


Figure 21: Board 1, VCF: (a) T7, self-oscillation frequency versus CV_{CUT} with a straight-line fit, the S3 −3 dB cutoff and the S3 self-oscillation frequency at 2.5 V; (b) T6, self-oscillation amplitude versus CV_{RES} at the 1 kHz cutoff code; (c) T8, response at the harmonics of a 110 Hz saw (filtered relative to the open filter) with a 4-pole fit.

show a similar floor, about 55 dB below the signal peaks in a 24 kHz bandwidth. Two discrete lines appear in Figure 23: the running DCO's frequency and harmonics with all waveforms switched off and $CV_{AMP} = 0$ (feed-through with the VCA and filter open, up to −59 dB), and a line at 3125 Hz in every capture, the 46.875 kHz PWM and interrupt rate aliased by the 10 kS/s capture.

Sound examples recorded from the line output with the oscilloscope (demo tunes, waveform switching and the self-oscillating filter played as a scale) are in `docs/audio/hw_board1/`.

11.4 Calibration and validation

- **Calibration (L3)**: the calibration stores the DCO gain (expected 0.95–1.05), the cutoff scale and offset (from the self-oscillation frequency at two CV codes), the VCA trim code (expected 30–230) and per-pad touch baselines and thresholds. The flash store is not implemented yet. Board 1 values found manually: VCA trim code 104, HSI clock −0.80 % (pitch −14 cent); the DCO amplitude is within −0.9 / +1.2 % without a gain constant. The touch baselines and thresholds are measured at every boot.
- **Validation (L4)**: covers reliable playing without ghost or double triggers, latency below 10 ms, tuning stability, usability of the parameter UI, the sound compared with the behavioural-model examples, the demo tunes, hum with typical adapters, and MIDI.

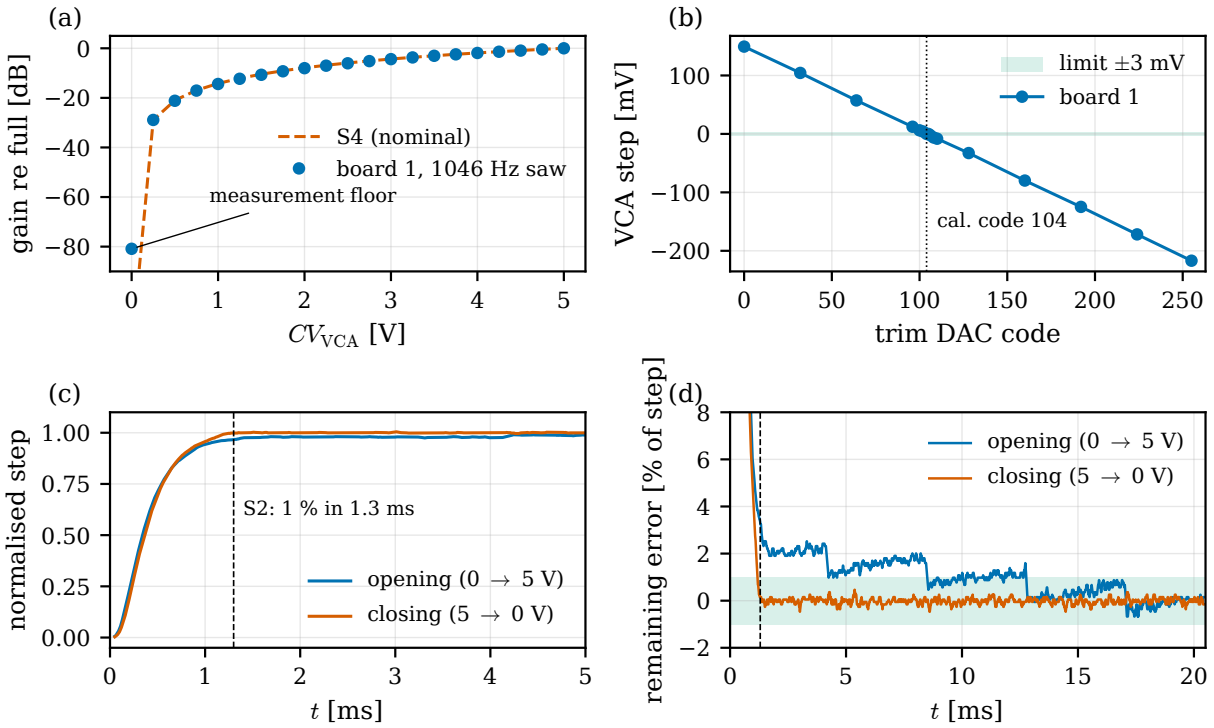


Figure 22: Board 1, VCA: (a) T9, gain law for a 1046 Hz saw against S4; (b) T10, DC step at VCAOUT when the VCA opens, versus trim code; (c) T11, CV_{VCA} step response at VCAOUT (trim 255 for a 220 mV DC step, 9-sample average), with the S2 settling time; (d) the same as remaining error.

Table 18: Traceability from requirements to simulation and hardware tests.

Requirement	Simulation	Hardware test
DCO range and amplitude ±5 %	S1	T4, T5
CV ripple and settling	S2	T11
VCF range, slope, resonance	S3	T6, T7, T8
VCA attenuation, thump	S4	T9, T10
Touch sensitivity and scan rate	S5	T2, T3, V1, V2
Complete voice	S6	V5
Power, hum	S7	B2–B5, T12, V6

12 Open points and risks

- **Accepted limitations.**
  - Power-on pop at the line output (about 3 V, 0.3 s).
  - Filter cutoff temperature drift of about −13 cent/K. It could be compensated in firmware by re-tuning from the self-oscillation frequency, measured through the loopback.
- **Not modelled in simulation.**
  - The TL072 input common-mode limit. The design keeps all TL072 inputs at or above 4 V.
  - Noise. Board 1 measures about −55 dB broadband, at the limit of the loopback (T12).
  - Transistor mismatch beyond the explicit cases.
  - Thermal effects in the VCA pair: board 1 shows a slow 2 % tail when the VCA opens (T11).
  - PCB parasitics, including key-to-key coupling of the touch pads and switching noise from the LEDs and shift registers. These are covered by T2 and T12.
- **Open after board 1 bring-up** (Section 11.3).
  - **Calibration store (L3).** Not implemented. The firmware boots with trim code 128,

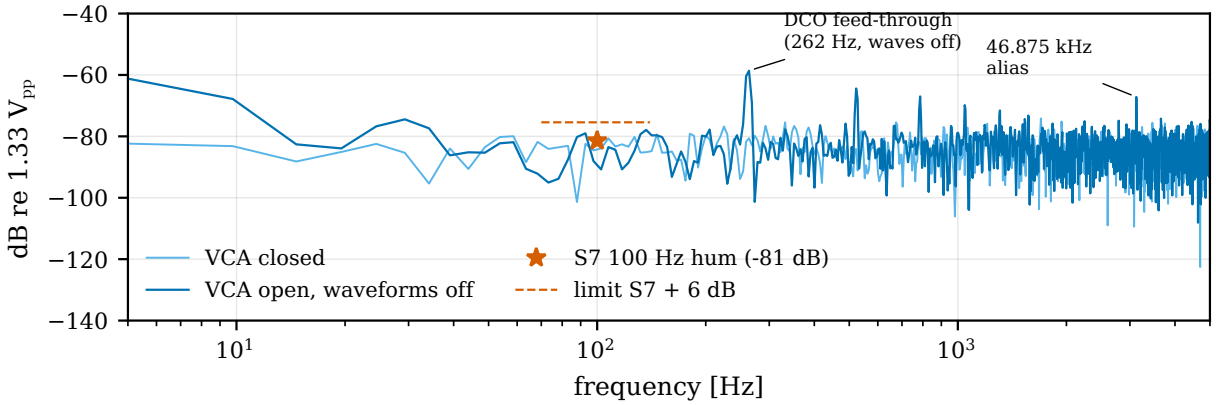


Figure 23: Board 1, T12: spectrum at VCAOUT (205 ms capture, 10 kS/s, Hann window), VCA open and closed, filter open, all waveforms off; the S7 hum value is for 200 mV_{pp} input ripple.

which leaves a 33 mV thump on board 1 (calibrated code 104). The pitch is 14 cent flat from the −0.80 % HSI error, and the HSI drifts by up to 0.1 %. The cutoff offset (about 0.1 octave against S3) is not stored either.

- **Noise margin.** The broadband floor of about −55 dB misses the −60 dB goal, but the 12-bit loopback cannot resolve it (quantisation alone −58 dB). It should be measured at the line output with an audio interface.
- **VCA opening tail.** The level creeps by about 2 % over 10 … 15 ms after the fast part of the step, most likely thermally. Expected to be inaudible; confirm by listening (V5).
- **DCO feed-through.** With all waveforms off and the VCA open, the DCO frequency is still visible at up to −59 dB.
- **Not yet tested.** B12 at 12 V, T3 (scan rate), T14 (MIDI), the on-chip `selftest`, hum with mains adapters (V6) and the L4 validation in general.
- **DAC mode** (Section 10.5). A faint 122 Hz line (the buffer-half rate, −61 dB re peak), probably the DSP's current bursts on the supply; smaller buffer halves would move it up and spread the load. The kettle uses up to about half of the CPU and leaves 1.4 KB of stack, so more digital voices need care. A firmware routine that blocks the main loop for more than a buffer half (8.2 ms) would starve the DAC; a console exchange does (about 20 ms).
- **For a board revision: PWM carrier crosstalk.** In DAC mode about 5.8 mV of the 93.75 kHz carrier reaches the line out past the filter and the VCA (Section 10.5). Inaudible, but it folds into the audio band of sampled recordings and can upset amplifiers or converters downstream. Slow the PULSE edges at the pin (series resistor and a small capacitor to ground, corner well above the carrier), and review the routing and ground return of the PULSE trace and its neighbours to the output stage. The firmware keeps the 93.75 kHz carrier for now; a higher carrier (375 kHz, 6-bit, still centred, interpolated and noise-shaped) would fold outside the audio band, but needs the DMA refill moved into an interrupt.

- **Touch sensitivity on the 4-layer board** (resolved on board 1). Real touches give 486 to 4233 counts against an untouched σ of 20–43 counts. The thresholds need a floor of 200 counts and a two-scan debounce, because the boot-time noise estimate is sometimes too low (Section 11).
- **CH32V006 pinout** (resolved). The V006 datasheet (V2.0, table 2-1-1, V006F8P7) gives the same TSSOP-20 pin numbers and the same `_2` remap functions as the CH32V002. The reset pin is PD7; PA4 is bonded to PD7 inside the package and is never used. Board 1 carries a CH32V006.
- **Assembly.** Check the orientation of the SOT-23/SOT-363 transistors, the diode and the

LEDs at the first inspection. Hand-solder the TSSOP-20 MCU and check pins 1–2 (PD4/PD5) for a bridge: board 1 had one, which held the loopback input low.

- **Documentation.** The specification (`docs/spec.md`) and the verification plan still describe some pre-layout details (two layers, test pads on the bottom side). This report reflects the design as ordered.

A Schematic

The following pages reproduce the KiCad schematic (`docs/touchsynth_schematic.pdf`) scaled to A4. The PDF is vector graphics and can be zoomed.

TouchSynth – MCU-controlled analog mono synth (CH32V003/V002)

power

Power, references and ladder bias

Datei: power.kicad_sch

mcu

MCU, programming header and MIDI in

Datei: mcu.kicad_sch

touch_led

Touch pads, multiplexers, LEDs and trim DAC

Datei: touch_led.kicad_sch

vcf

CV_CUT, expo converter, ladder filter, mixer

Datei: vcf.kicad_sch

resonance

CV_RES and resonance VCA

Datei: resonance.kicad_sch

vca

CV_VCA, VCA, line out and audio loopback

Datei: vca.kicad_sch

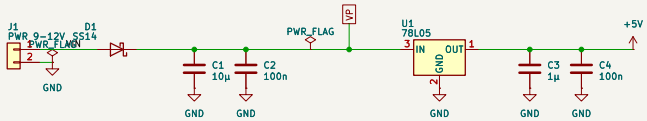
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Title: TouchSynth

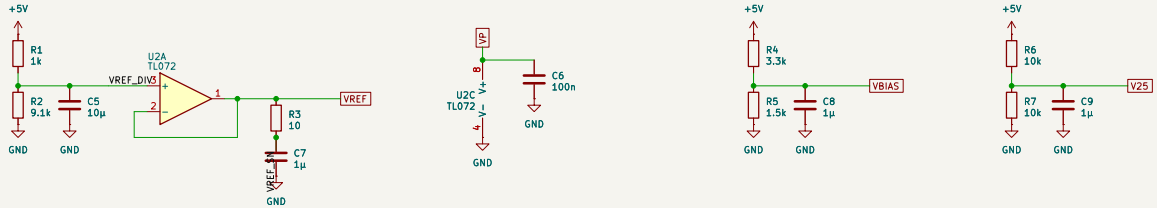
Size: A4	Date: 2026-09-27	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 1/8

Power, references and ladder bias

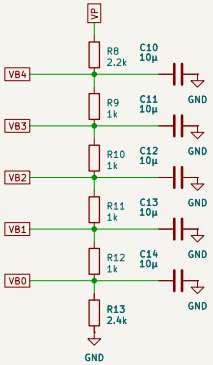
Input, reverse protection, 5 V



References: VREF 4.5 V (buffered), VBIAS 1.5 V, V25 2.5 V



Ladder bias chain (from V+; VB0…VB4 = 2.4…6.4 V at V+ = 8.6 V)



Test points



Generated by hw/gen_sch2.py (layouts.py) from hw/design.py

Sheet: /power/
File: power.kicad_sch

Title: TouchSynth — Power, references and ladder bias

Size: A3	Date: 2026-09-27	Rev: 0.1
KiCad E.D.A. 10.0.6		Id: 2/8

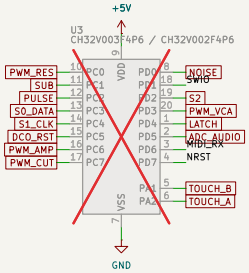
TouchSynth — design report

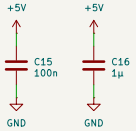
rev 0.1

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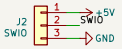
MCU, programming header and MIDI in

MCU: CH32V003F4P6 or CH32V002F4P6 (TSSOP-20, hand-soldered, not placed by JLCPCB)



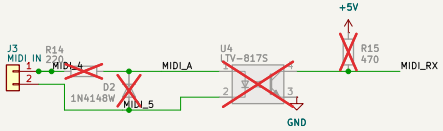


Programming (WCH-LinkE, SWIO)





MIDI in (not populated in rev 0.1)



TouchSynth — design report

rev 0.1

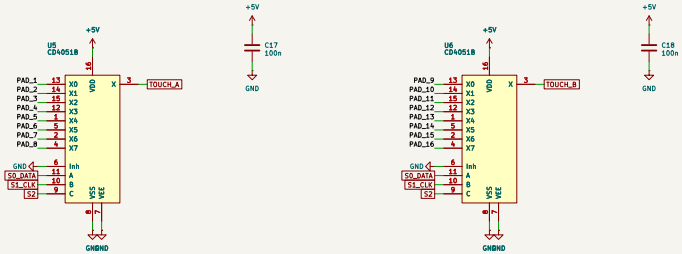
38

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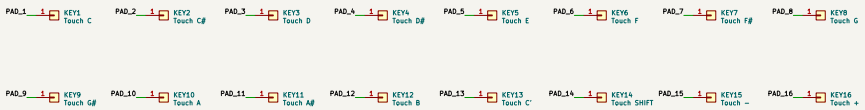
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Size: A3	Date: 2026-09-27	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 3/8

Touch pads, multiplexers, LEDs and trim DAC

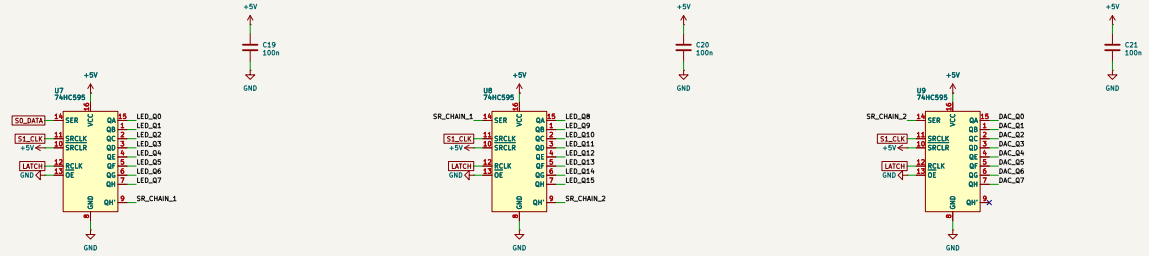
Touch multiplexers (select S0…S2 shared with the 74HC595 data / clock)



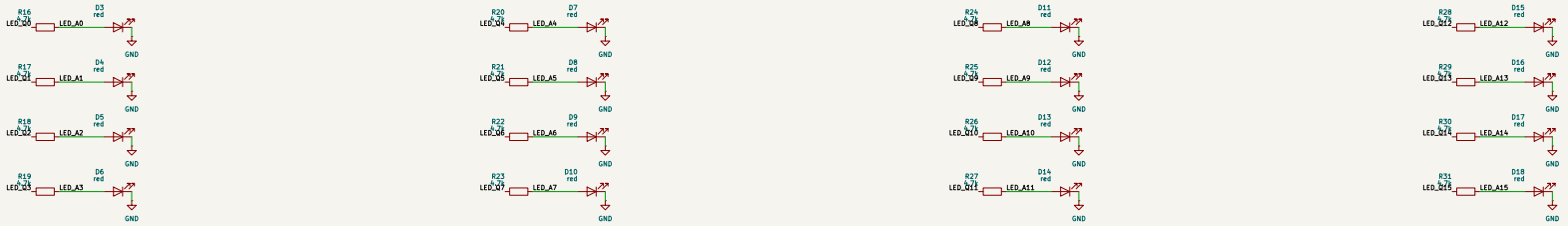
Touch pads (copper under solder mask)



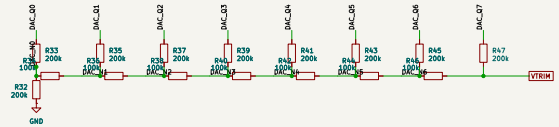
Shift registers (daisy-chained: LEDs 0–7, LEDs 8–15, trim DAC)



LEDs (4.7k series resistors, ~0.6 mA each)



VCA trim DAC: 8-bit R-2R ladder (R = 100k, 2R = 200k), output impedance 100k



TouchSynth — design report

rev 0.1

Generated by hw/gen_sch2.py (layouts.py) from hw/design.py

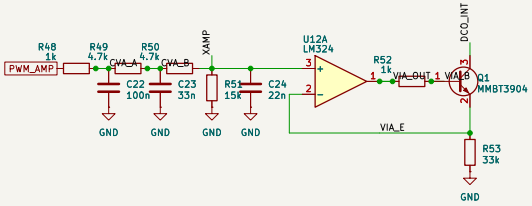
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Size: A2	Date: 2026-09-27	Rev: 0.1
KiCad E.D.A. 10.0.6		Id: 4/8

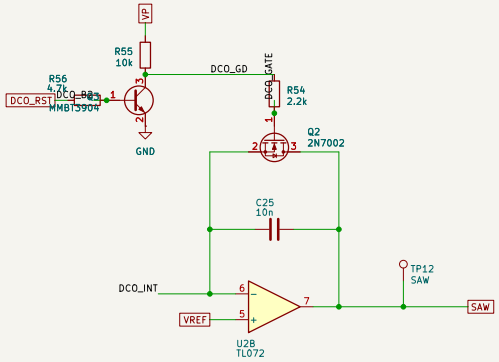
DCO and CV_AMP

CV_AMP: PWM filter and V−to−I converter (charge current proportional to the note frequency)





Integrator (TL072) with 2N7002 reset and NPN gate level shifter



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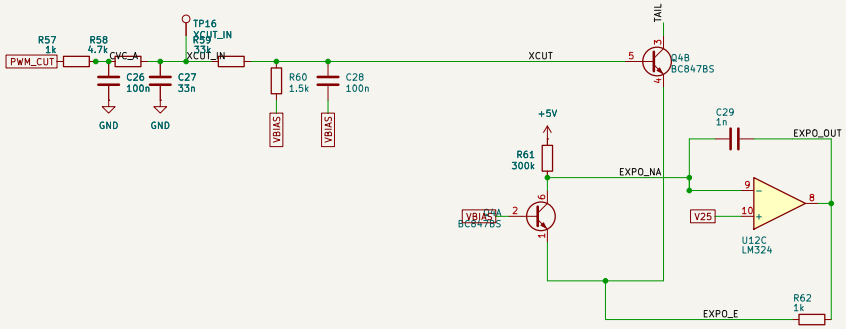
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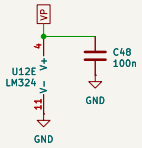
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KiCad E.D.A. 10.0.6		Id: 5/8

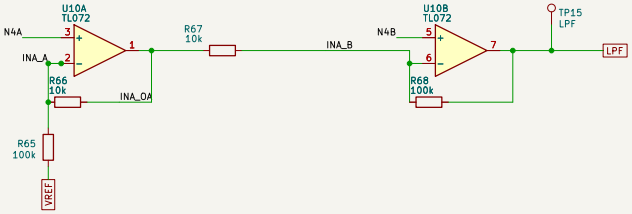
CV_CUT, expo converter, ladder filter, mixer

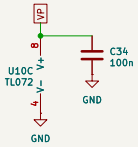
CV_CUT: PWM filter and exponential converter (tail current of the ladder)



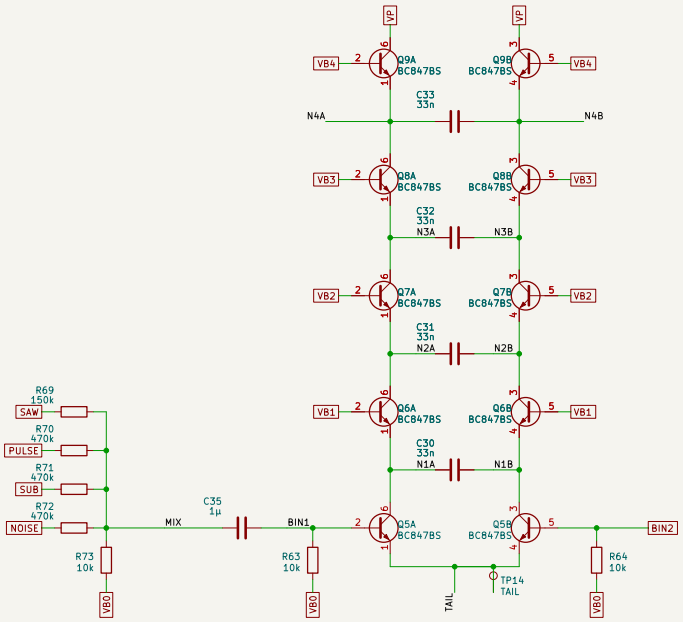


Output instrumentation amplifier across the top capacitor (G = 11, referenced to VREF)





Transistor ladder (4 poles, 4 x 33 nF), bias from VB0...VB4, mixer

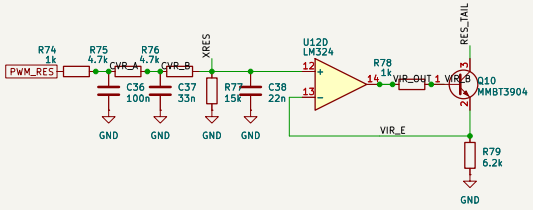


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Size: A3	Date: 2026-09-27	**Rev: 0.1**
KiCad E.D.A. 10.0.6		Id: 6/8

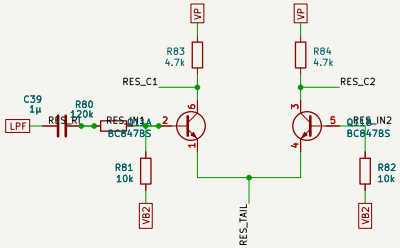
CV_RES and resonance VCA

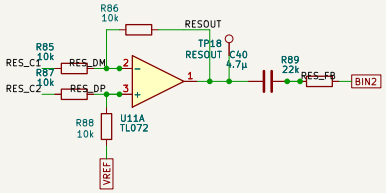
CV_RES: PWM filter and V−to−I converter (tail current of the resonance VCA)





Resonance VCA: differential pair, difference amplifier, AC−coupled feedback into the ladder (BIN2)





Generated by hw/gen_sch2.py (layouts.py) from hw/design.py

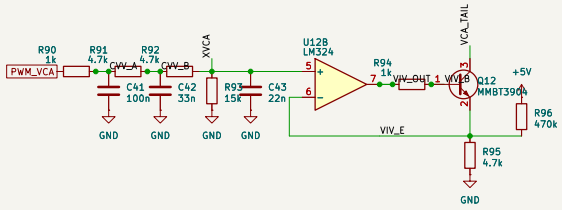
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Title: TouchSynth — CV_RES and resonance VCA

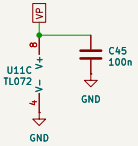
Size: A3	Date: 2026-09-27	Rev: 0.1
KiCad E.D.A. 10.0.6		Id: 7/8

CV_VCA, VCA, line out and audio loopback

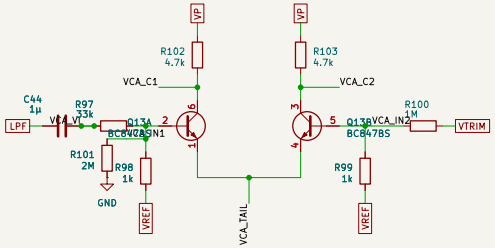
CV_VCA: PWM filter and V−to−I converter (470k pull−up guarantees zero current at CV = 0)

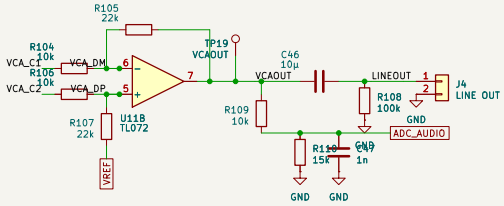






VCA: differential pair with offset trim, difference amplifier, line out, audio loopback





Generated by hw/gen_sch2.py (layouts.py) from hw/design.py

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File: vca.kicad_sch

Title: TouchSynth — CV_VCA, VCA, line out and audio loopback

Size: A3	Date: 2026-09-27	Rev: 0.1
KiCad E.D.A. 10.0.6		Id: 8/8

B Reproducing the design

```
cd sim/s1_dco && python s1_dco.py      # likewise s2_cv ... s8_dac (order: S1, S3, S4, S6)
cd sim/behav && python validate.py && python examples.py
cd hw && python gen_sch2.py && python check_netlist.py && python check_sim.py
cd hw && <KiCad python> gen_pcb.py --route  # placement, routing, fill, stitching
cd hw && python fab.py                      # gerbers, BOM, CPL
cd docs/report && python gen_tables.py && latexmk -pdf touchsynth_report.tex
cd firmware/touchsynth && python gen_tables.py && make TARGET_MCU=CH32V006 && make flash
# bench (lab setup in tools/lab.conf, from tools/lab.conf.example):
cd tools && python hwtest.py dco      # also vcf, vca, settle, hum, lpf
cd tools && python hw_figures.py && python instrument_figures.py <timpani recording>
./record_parts.sh 200 march_timp:15   # on the lab PC: one part per take
cd tools && python mix_parts.py hw <takes> march && python suite.py hw <takes>
```